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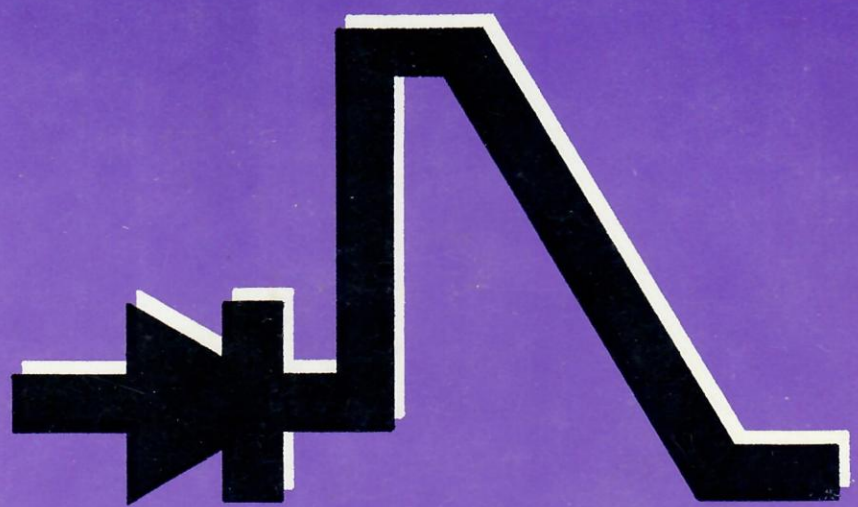
PULSES & WAVESHAPING BOOK V

CES INDUSTRIES, INC.

Ed-Lab

EXPERIMENT MANUAL

PULSES & WAVESHAPING BOOK V



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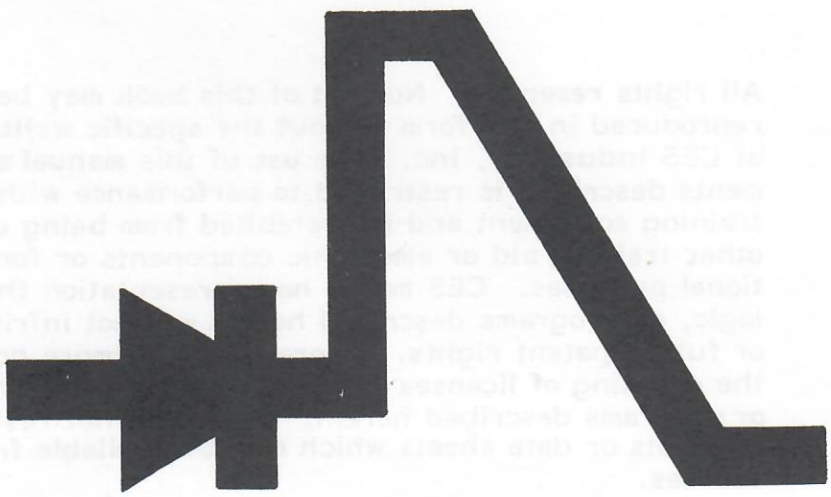

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EXPERIMENT MANUAL

PULSES & WAVESHAPING

BOOK V

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ISBN 0-86711-052-X
Printed in United States of America

PREFACE

The most important Pulse is your HEARTBEAT, also called your PULSE. Other obvious electrical pulses include the telephone dialing pulses which direct your call to one of millions of other telephones, the automobile ignition system which shapes and directs pulses to each of the eight spark plugs, and control and data pulses in commercial calculators, digital clocks, and computers to control, calculate, and display information. Television uses electronics pulse detection and shaping circuits to provide signals for the TV screen synchronization and intensity modulation.

Other large system applications where pulse circuits are vital include Radar, Navigation, Sonar, and other military applications for Fire Control, Missile Guidance, Aircraft Control and so on.

This unit of study covers the broadest variety of circuits for Pulse Generation, Characteristics, Measurement, Time Constants, and Multivibrator Oscillators. The next group of circuits demonstrate how Resistors, Capacitors, and Inductors provide Passive Waveshaping. Transistor Circuits, Vacuum Tube Circuits, and Integrated Circuits provide Active Waveshaping. Active Sweep Circuits, Logic Circuits, and Pulse Drivers demonstrate additional basic concepts and techniques, and furnish the experience necessary to understand and develop a capability in this important aspect of electronics.

The entire Ed-Lab program, as well as this series of Pulse and Waveshaping Electronics circuits, is designed to be self-contained and easy and motivating for learning, and directly suitable for Individual Instruction and Self-Paced Study. Students can proceed from one subject to another at their own rates. These most interesting and widely used topics in electronics can be covered easily, and quickly, to provide the student with the added knowledge and skills which can result in a broader opportunity to achieve more occupational successes.

Norman Nesenoff
President
CES INDUSTRIES, INC.
Farmingdale, New York

Safety is good common sense. The Ed-Lab equipment is designed with all current limited and voltage limited Power Supplies so that there is no danger to the student when touching any wires and no danger of burning-out any of the electronic components.

DO NOT USE AN EXTERNAL POWER SUPPLY WITH THE ED-LAB.

While working in the laboratory, the student is exposed to many different types of equipment, power tools, soldering irons, test equipment, drills, rotating machinery, and so on. The 120 volt power socket can cause a shock, and the shock can result in your jumping or falling. Care should be exercised while working on any equipment including automobiles, television sets, carpentry tools, as well as electricity and electronics.

Do not get involved in any "horsing-around" or in practical jokes. Don't throw anything in the lab. Don't drop the equipment off the bench or on your foot. Don't burn the line cord with a soldering iron. If you remove the Ed-Lab front panel, don't touch the 120 volt line-cord connections in the rear while the plug is still connected to the socket.

If an accident occurs, notify your instructor, shut off all power, and administer first aid as necessary. Your instructor should review with you the safety requirements in your laboratory.

Ed-Lab

FIRST AID for ELECTRICAL SHOCK

If you observe an accident involving electrical shock,
DON'T JUST STAND THERE - DO SOMETHING!

RESCUE OF SHOCK VICTIM

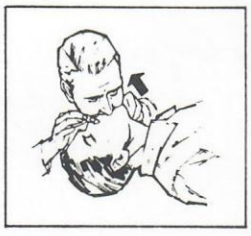
The victim of electrical shock is dependent upon you to give him prompt first aid. Observe these precautions:

1. Shut off the high voltage.
2. If the high voltage cannot be turned off without delay, free the victim from the live conductor. REMEMBER:
   a. Protect yourself with dry insulating material.
   b. Use a dry board, your belt, dry clothing, or other non-conducting material to free the victim. When possible PUSH - DO NOT PULL the victim free of the high voltage source.
   c. DO NOT touch the victim with your bare hands until the high voltage circuit is broken.

FIRST AID

The two most likely results of electrical shock are: bodily injury from falling, and cessation of breathing. While doctors and pulmotors are being sent for, DO THESE THINGS:

1. Control bleeding by use of pressure or a tourniquet.
2. Begin IMMEDIATELY to use artificial respiration if the victim is not breathing or is breathing poorly:
   a. Turn the victim on his back.
   b. Clean the mouth, nose, and throat. (If they appear clean, start artificial respiration immediately. If foreign matter is present, wipe it away quickly with a cloth or your fingers).



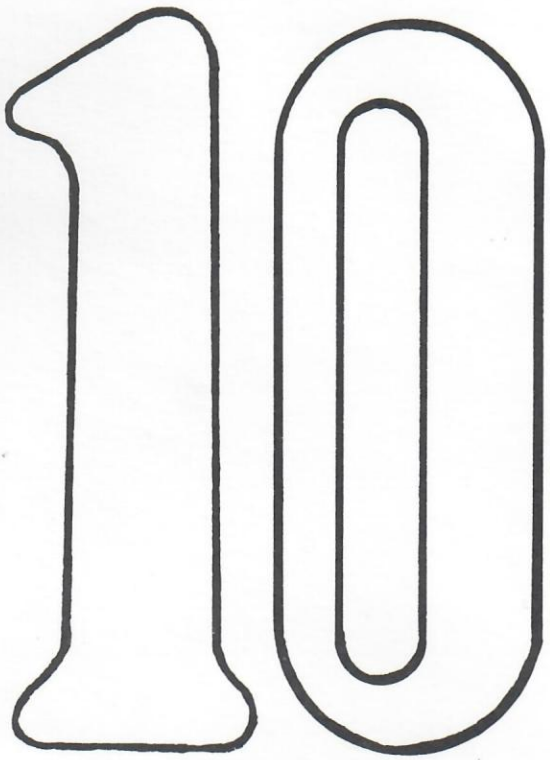
   c. Place the victim's head in the "sword-swallowing" position. (Place the head as far back as possible so that the front of the neck is stretched).
   d. Hold the lower jaw up. (Insert your thumb between the victim's teeth at the midline - pull the lower jaw forcefully outward so that the lower teeth are further forward than the upper teeth. Hold the jaw in this position as long as the victim is unconscious).
   e. Close the victim's nose. (Compress the nose between your thumb and forefinger).
   f. Blow air into the victim's lungs. (Take a deep breath and cover the victim's open mouth with your open mouth, making the contact air-tight. Blow until the chest rises. If the chest does not rise when you blow, improve the position of the victim's air passageway, and blow more forcefully. Blow <u>forcefully</u> into <u>adults</u>, and <u>gently</u> into <u>children</u>.
   g. Let air out of the victim's lungs. (After the chest rises, quickly separate lip contact with the victim allowing him to exhale).
   h. Repeat steps f. and g. at the rate of 12 to 20 times per minute. Continue rhythmically without interruption until the victim starts breathing or is pronounced dead. (A smooth rhythm is desirable, but split-second timing is not essential).

DON'T JUST STAND THERE - DO SOMETHING!

Ed-Lab

EXPERIMENT MANUAL

PULSES & WAVESHAPING



UNIT NO.

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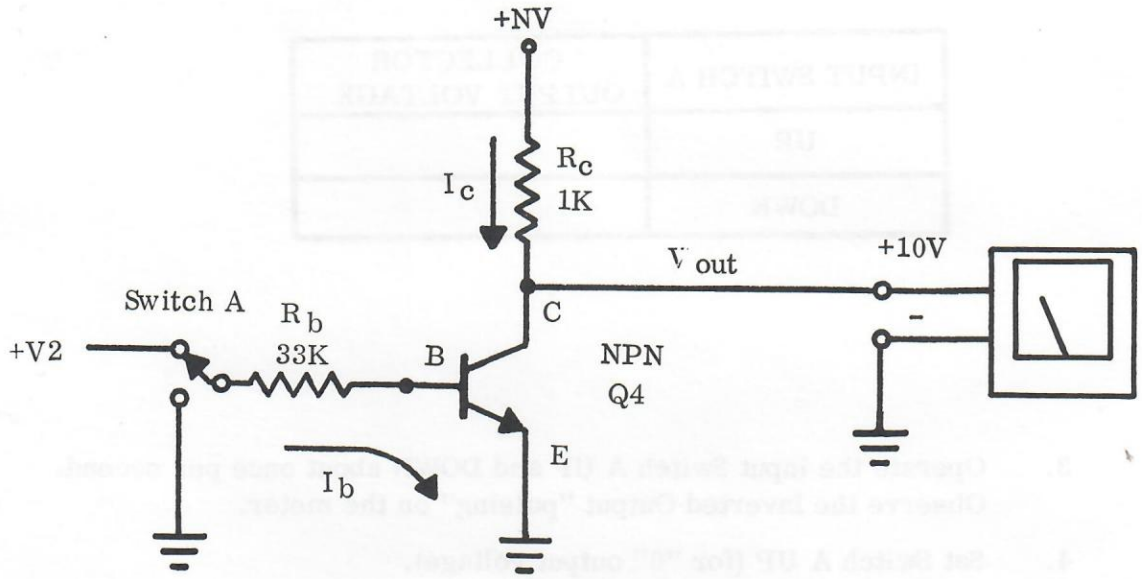


Figure 1-1 Transistor Switch

Objective:

You will apply a switched input to a TRANSISTOR base (input) and you will observe the inverted PULSE output (collector).

Description:

When the input Switch A is "UP", a positive voltage and current are applied to the transistor base and current (I_b) flows in the transistor Base-Emitter Circuit. The transistor is "switched-ON" and current (I_c) flows through the transistor with a collector output voltage of "0" volts.

When the input Switch A is down to "0" volts, there is no input current and the transistor is OFF. The output collector voltage is + volts or approximately +10 volts. The output voltage is the "opposite" of the input voltage and this Transistor Switch Circuit is called an INVERTER.

Procedure:

1. Wire the circuit in Figure 1-1.
2. Operate the input Switch UP and DOWN and record the output voltages.

INPUT SWITCH A	COLLECTOR OUTPUT VOLTAGE
UP	
DOWN	

3. Operate the input Switch A UP and DOWN about once per second. Observe the Inverted Output "pulsing" on the meter.
4. Set Switch A UP (for "0" output voltage).
5. Change the meter lead from the +10 volt scale to the +0.5 volt scale. Read the output voltage.

ACTUAL OUTPUT "ZERO" VOLTS =

Exercises:

1. Substitute the Silicon Transistor (Q7) and repeat step 5 to measure the ON Saturation Voltage.

ZERO VOLTS OUTPUT (SILICON) =

Ed-Lab	BISTABLE MULTIVIBRATOR	EXP. NO. 2 Page No. 1

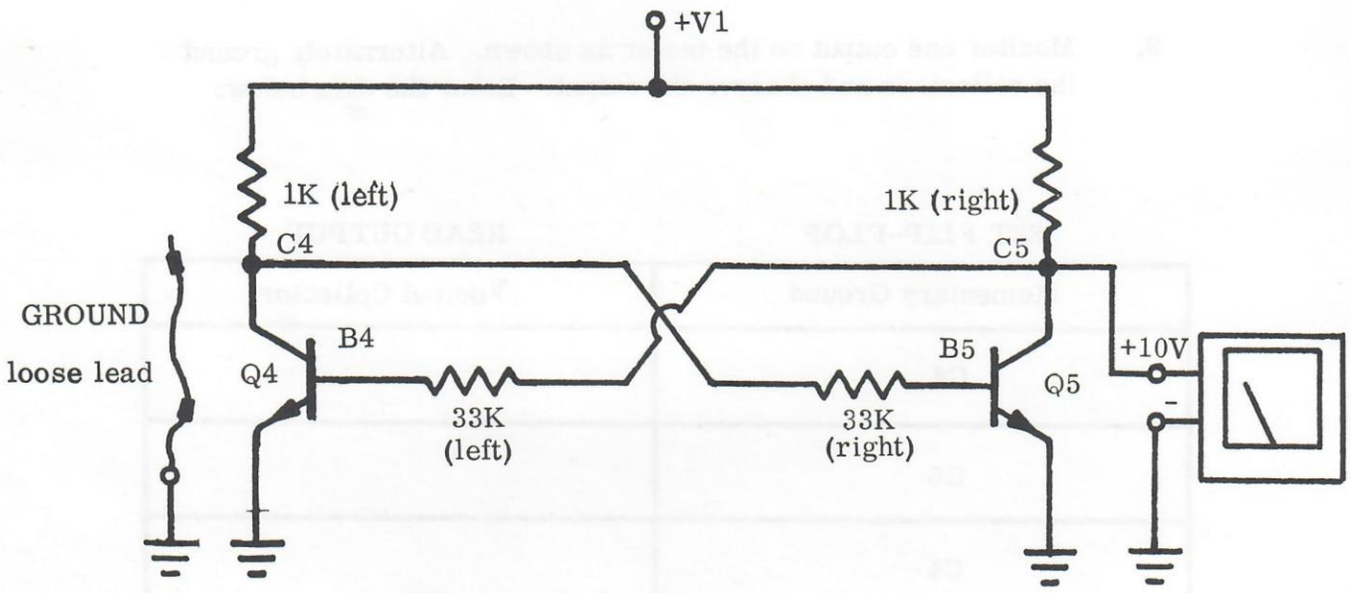


Figure 2 - 1 Bistable Multivibrator

Objective:

You will use two transistor "pulse inverters" connected together; each output to the other input. You will observe that the circuit has "two-stable" conditions.

Description:

When the first collector (C4) is "high" at a positive voltage, transistor Qt is ON and the output is low. Either collector can be forced to "ground" or low by "grounding" that COLLECTOR or the opposite BASE using a loose lead as shown. Such a circuit has two possible stable or steady conditions and is called a BISTABLE MULTIVIBRATOR or "FLIP-FLOP".

Procedure:

1. Wire the circuit in Figure 2 - 1.

2. Monitor one output on the meter as shown. Alternately ground the collectors and observe the output. Enter the data below:

SET FLIP-FLOP	READ OUTPUT
Momentary Ground	$V_{output\ Collector}$
C4	
C5	
C4	
C5	
B4	
B5	
B4	
B5	

Question:

1. What is the output voltage on collector C4 when the voltage on C5 is zero volts?

Ed-Lab | CAPACITOR PULSER | EXP. NO. 3 Page No. 1

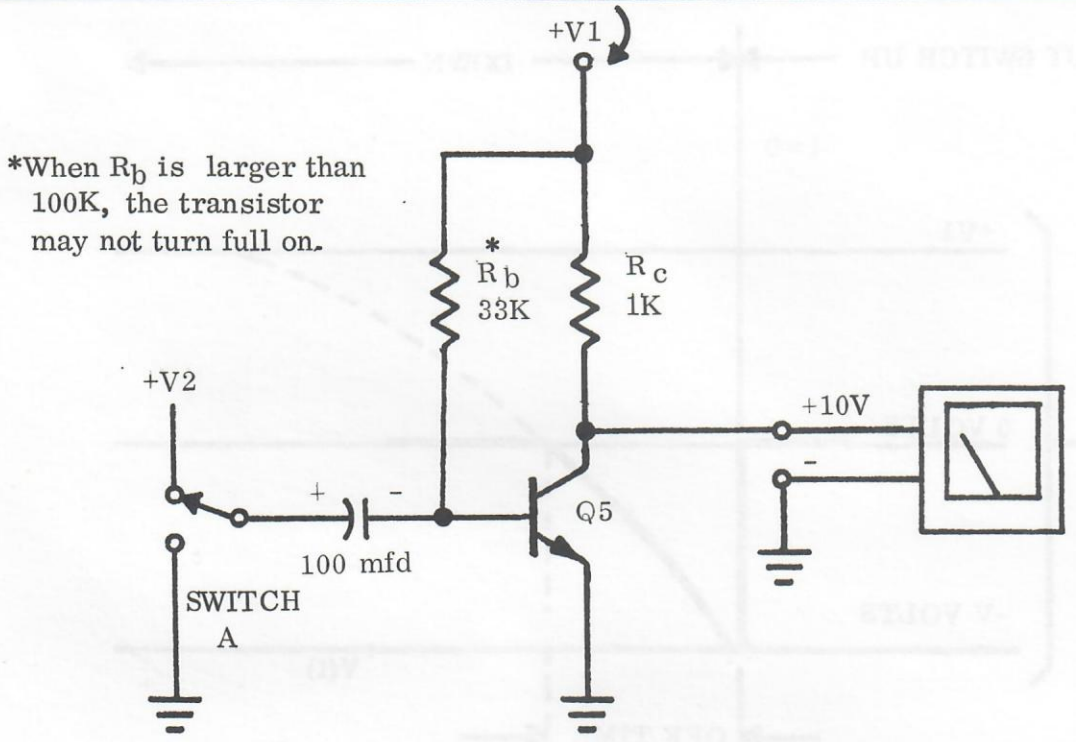


Figure 3 - 1 One-Shot Pulser

Objective:

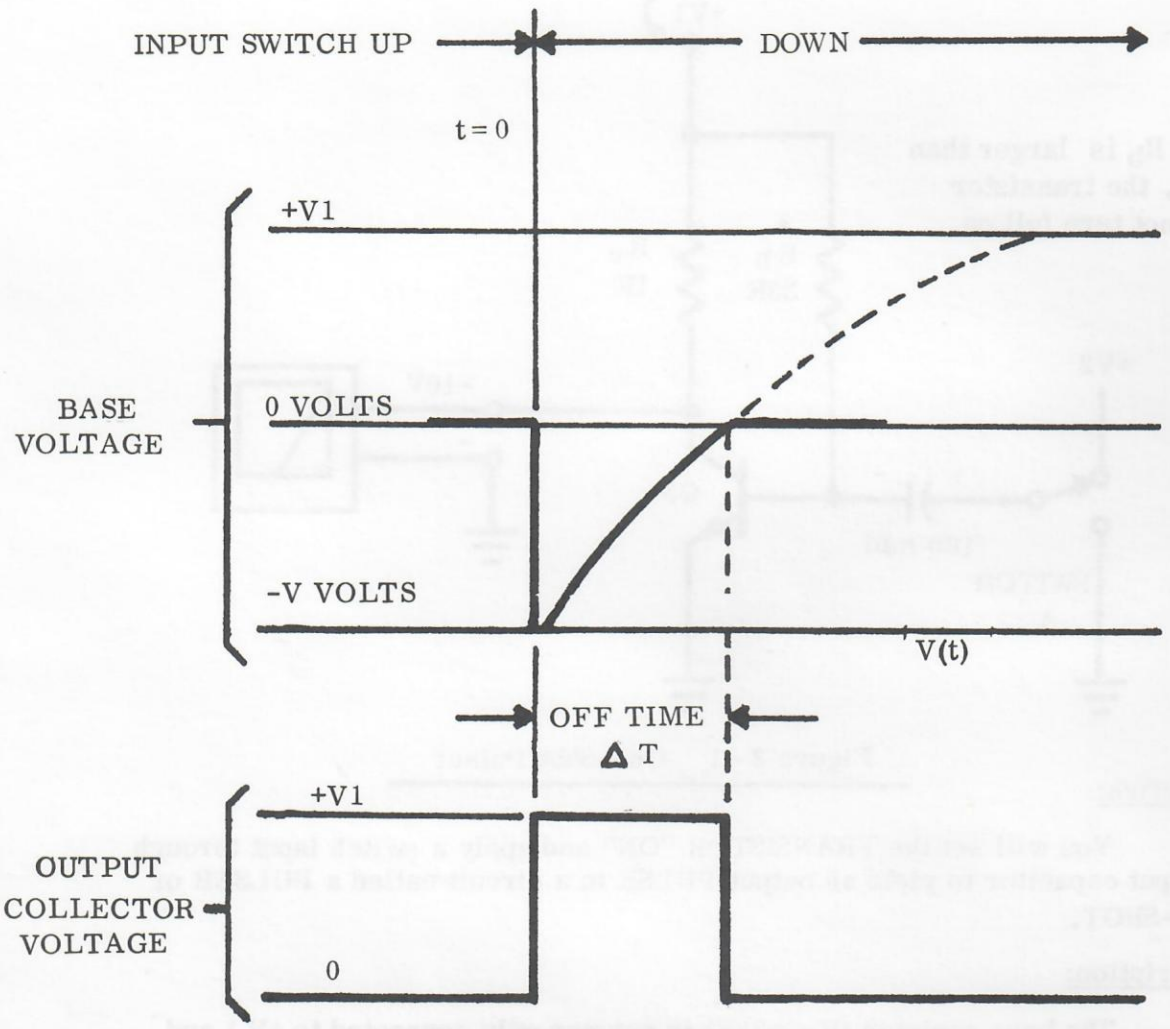
You will set the TRANSISTOR "ON" and apply a switch input through an input capacitor to yield an output PULSE in a circuit called a PULSER or ONE-SHOT.

Description:

The base resistor (R_b = 33K) is permanently connected to +V 1 and the transistor is "ON" with a collector voltage of $V_c = 0$. When the input Switch A is switched DOWN, a negative "step" input is applied to the capacitor (-10 volts). The voltage "across" a capacitor cannot change quickly and thus the entire input negative switching input is applied to the transistor base (-10 volts) and the transistor is "CUT-OFF". The output collector voltage V_c becomes +10 volts.

The base voltage "charges-up" from -10 volts through the base resistor (R_b) to +10 volts, (charging circuit is R_b and C), and when 0 volts (or approximately +0.3 volts) is reached, the transistor is "turned-on" and the output collector voltage V_c becomes "zero" again. Nothing happens to the output voltage when the switch is set UP, but the capacitor is charged to a positive voltage through the base-emitter circuit.

The output pulse starts when the switch is set DOWN. The output pulse is then "UP" for a "time" or "duration" or "width" which is determined by the R_b, C circuit as shown.



The equation for the waveform is:

$$V(t) = V - 2V\, e^{-t/RC}$$

where V = 9 Volts

R = 33K = 33,000 ohms

C = 100 mfd = 100×10^{-6}

The pulse width (ΔT) is determined where V(t) = 0;

$$0 = V - 2V\, e^{-\Delta T/RC}$$

$$2\, e^{-\Delta T/RC} = 1$$

And calculating:

$$\Delta T = 3 \text{ seconds}$$

Procedure:

1. Wire the Circuit in Figure 3 - 1.
2. Operate the Input Switch A, and measure the Pulse Width.

INPUT: SWITCH A	OUTPUT: PULSE-WIDTH
UP THEN DOWN	

3. Substitute different values for R_b and C and measure the pulse widths.

   Input Switch A: UP then DOWN

R_b	C	Measure PULSE WIDTH

Questions:

1. What would the "pulse-width" be for R = 10K and C = 0.001 mfd?

Ed-Lab	ASTABLE MULTIVIBRATOR	EXP. NO. 4 Page No. 1

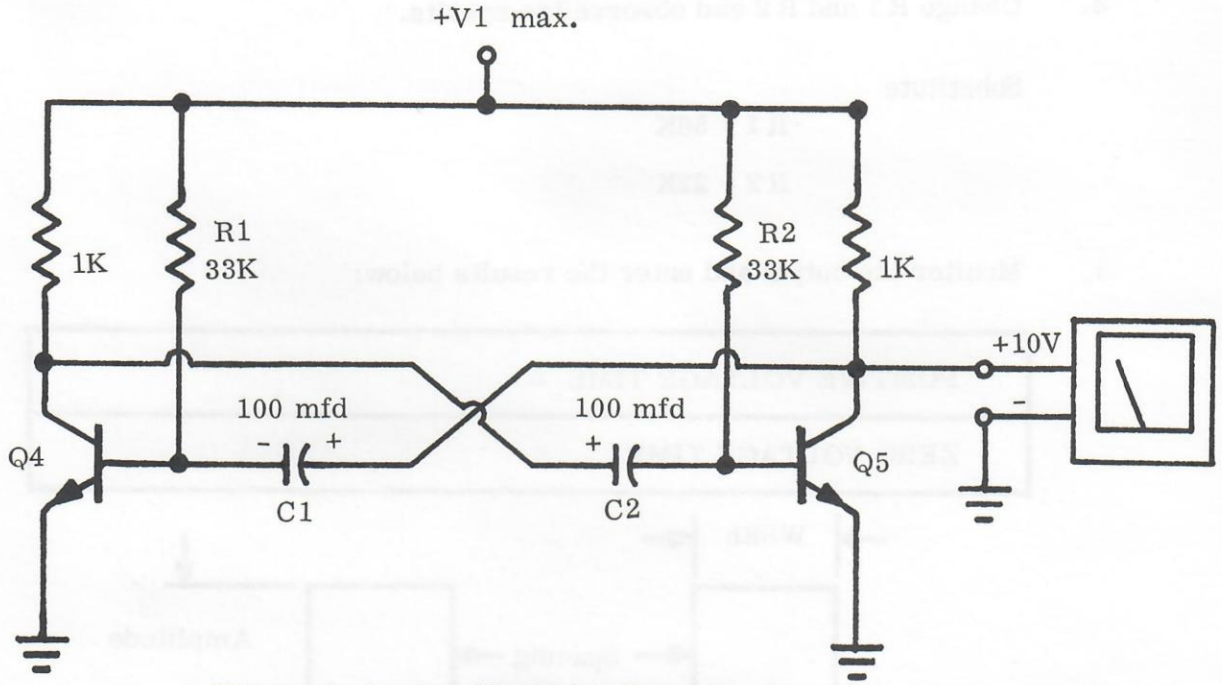


Figure 4 - 1 Astable Multivibrator

Objective:

You will connect two ONE-SHOT Pulsers "end-to-end" to result in an alternating pulse circuit or ASTABLE MULTIVIBRATOR.

Description:

Two ONE-SHOT pulsers from the previous experiment are connected together.

The output from one is connected to the input of the other, and they alternately pulse each other.

Procedure:

1. Wire the circuit in Figure 4 - 1.
2. Monitor the output and describe the output - (Voltage and Time).

OUTPUT

3. Change R 1 and R 2 and observe the results.

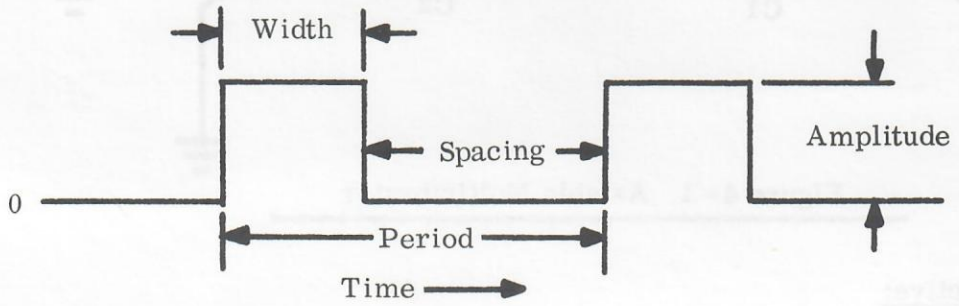
Substitute

R 1 = 56K

R 2 = 22K

4. Monitor the output and enter the results below:

POSITIVE VOLTAGE TIME =
ZERO VOLTAGE TIME =



5. The PERIOD is the sum of the ON and OFF time. Calculate:

PERIOD = seconds

6. The DUTY CYCLE is ratio of the Pulse Width to the Period.

$$\text{DUTY CYCLE} = \frac{\text{PULSE WIDTH}}{\text{TOTAL PERIOD}} \times 100\% =$$

Calculate the Duty Cycle for the results from the resistors in paragraph 2 and 3 above.

R 1 = R 2 = 33K Duty Cycle = _____

R 1 = 56K R 2 = 22K Duty Cycle = _____

7. The FREQUENCY can be calculated in Pulses per Second or Pulses per Minute. Calculate the FREQUENCY

(R 1 = R 2 = 33K) FREQUENCY = _____

(R 1 = 56K, R 2 = 22K) FREQUENCY = _____

Ed-Lab | MONOSTABLE MULTIVIBRATOR | EXP. NO. 5 Page No. 1

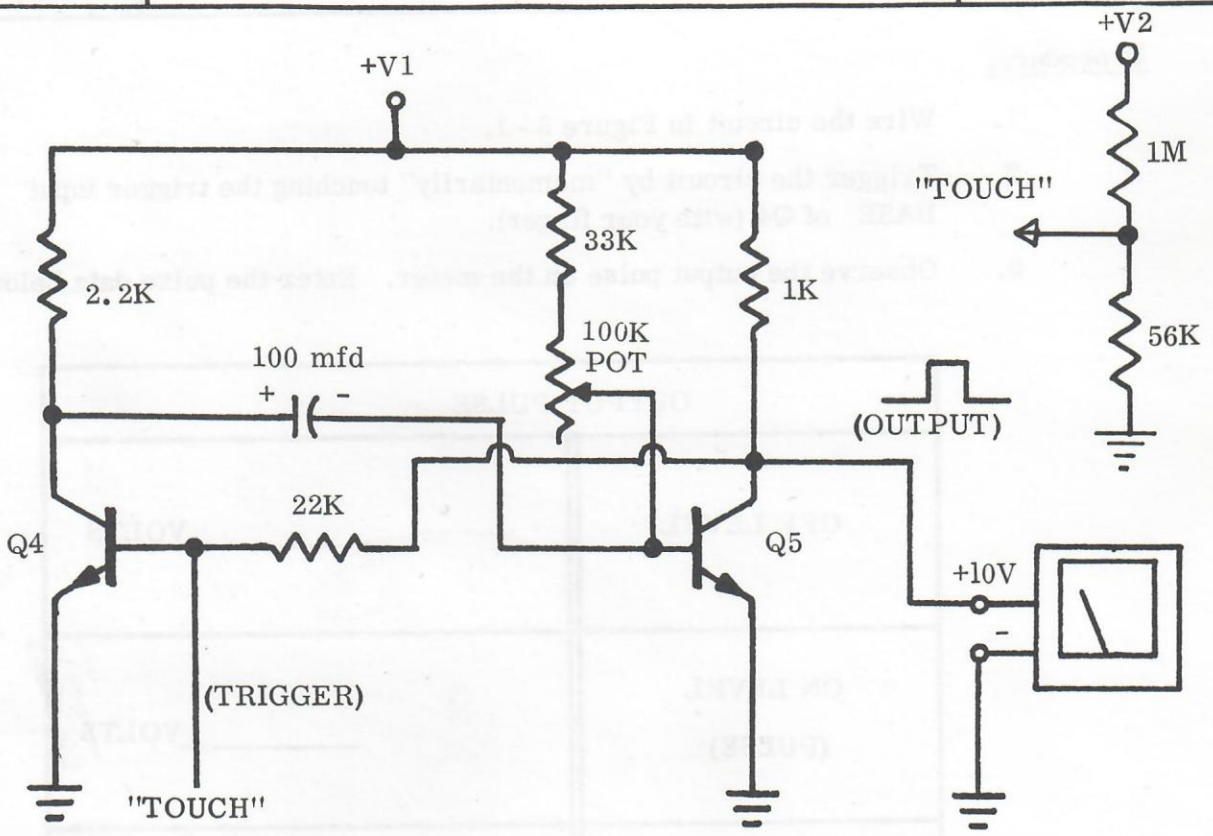


Figure 5-1 Monostable Multivibrator

Objective:

You will connect a ONE-SHOT PULSER and an INVERTER in a feedback loop to result in a sensitive ONE-SHOT circuit or MONOSTABLE MULTIVIBRATOR.

Description:

The MONOSTABLE MULTIVIBRATOR can be considered as an AMPLIFIER-INVERTER (Transistor Q4) as in the previous Experiment No. 1 connected to "drive" a ONE-SHOT PULSER (Transistor Q5) as in Experiment No. 3. The output from the One Shot Pulser is connected to the input (22K) of the INVERTER. We apply a very small "TRIGGER" input voltage to the Q4 Base.

The Inverter-Amplifier "amplifies" the trigger voltage which then "drives" the One-Shot. The positive voltage output from the One-Shot then drives the amplifier "further" ON via the 22K (feedback) resistor. The advantages of this circuit are that only a "small" trigger voltage is needed, and the feedback results in a "sharp" pulse rise and fall due to the feedback or "regeneration".

Procedure:

1. Wire the circuit in Figure 5 - 1.
2. Trigger the circuit by "momentarily" touching the trigger input BASE of Q4 (with your finger).
3. Observe the output pulse on the meter. Enter the pulse data below:

OUTPUT PULSE	
OFF LEVEL	_____VOLTS
ON LEVEL (PULSE)	_____VOLTS
ON TIME	_____ SECONDS

Ed-Lab | EMITTER COUPLED MULTIVIBRATORS | EXP. NO. 6 Page No. 1

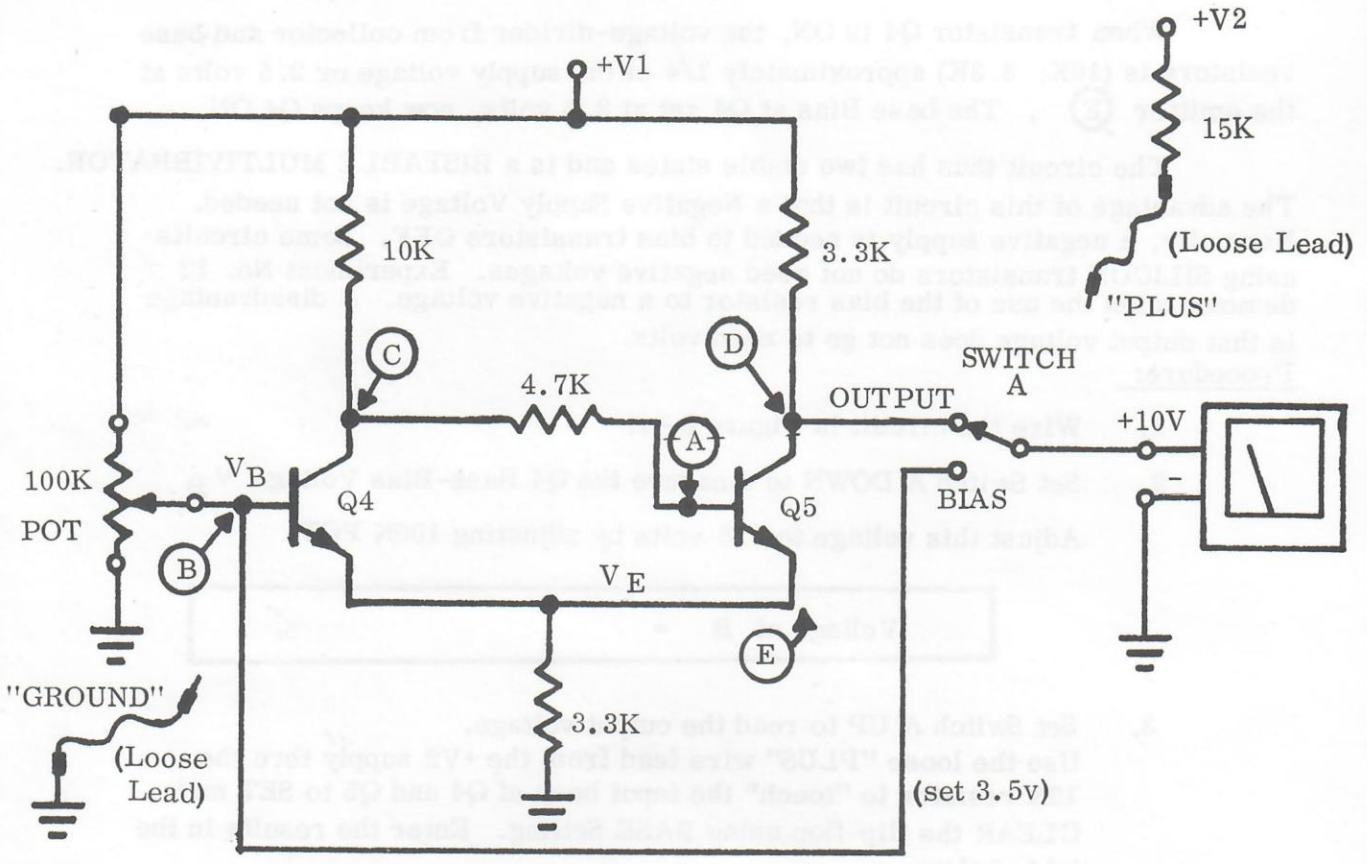


Figure 6 - 1 Emitter Coupled Bistable

Objective:

You will connect two amplifiers in a feedback circuit with EMITTER-COUPLING to result in an EMITTER COUPLED BISTABLE MULTIVIBRATOR.

Description:

A transistor amplifier (Q4) output (point C) is connected to another transistor (Q5) amplifier base input (point A). The "feedback" from this amplifier (Q5) to the first amplifier is by direct connection between the emitters or EMITTER COUPLING. When transistor Q5 is (switched) ON, the voltage divider between the (3.3K) collector resistor and the (3.3K) emitter resistor results in a voltage at the collector (D) and the emitter (E) of Q5 of approximately 4.5 volts (half of the 9 volt supply voltage +V1). Transistor Q4 is kept OFF by a lower base voltage at (B) which should be set at approximately 3.5V.

When transistor Q4 is ON, the voltage-divider from collector and base resistors is (10K; 3.3K) approximately 1/4 of the supply voltage or 2.5 volts at the emitter (E) . The base Bias at Q4 set at 3.5 volts, now keeps Q4 ON.

The circuit thus has two stable states and is a BISTABLE MULTIVIBRATOR. The advantage of this circuit is that a Negative Supply Voltage is not needed. Normally, a negative supply is needed to bias transistors OFF. Some circuits using SILICON transistors do not need negative voltages. Experiment No. 12 demonstrates the use of the bias resistor to a negative voltage. A disadvantage is that output voltage does not go to zero volts.

Procedure:

1. Wire the circuit in Figure 6 - 1.
2. Set Switch A DOWN to measure the Q4 Base-Bias Voltage V_B

   Adjust this voltage to 3.5 volts by adjusting 100K POT.

Voltage at B =

3. Set Switch A UP to read the output voltage.
   Use the loose "PLUS" wire lead from the +V2 supply thru the 15K resistor to "touch" the input base of Q4 and Q5 to SET and CLEAR the flip-flop using BASE Setting. Enter the results in the table below.

PLUS lead from +V2 (Momentarily connect to)	OUTPUT VOLTAGE (Switch A UP)
SET (B) (Base Q4)	
CLEAR (A) (Base Q5)	

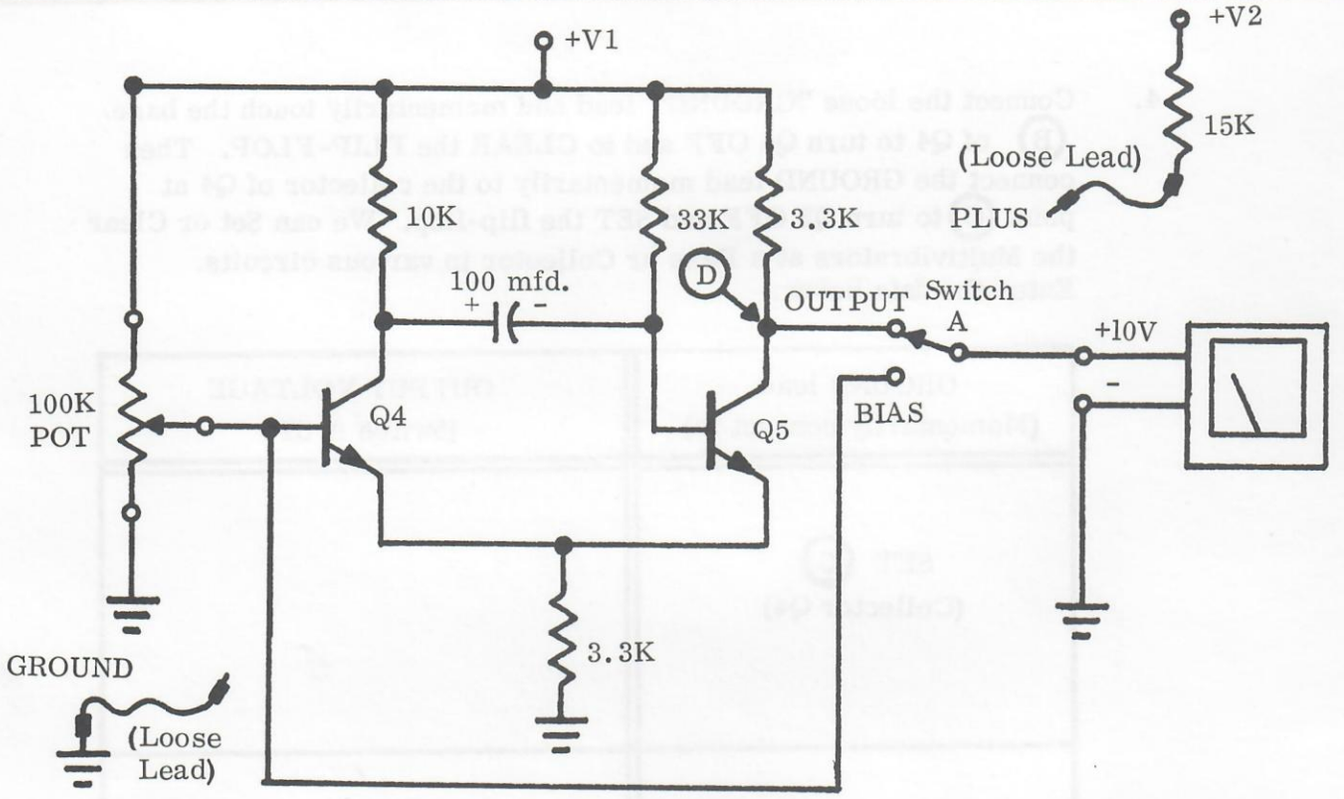


Figure 6 - 2. Emitter Coupled Monostable

6. After wiring the circuit in Figure 6 - 2. Set Switch A DOWN and check the adjustment of the bias at 3.5 volts.

   Set Switch C UP to observe the output (D) .

7. TRIGGER the MONOSTABLE MULTIVIBRATOR at the BASE of Q4 (with +V2) or at the COLLECTOR OF Q4 (with GROUND). Enter the data below:

TRIGGER	OUTPUT VOLTS (Switch A UP)
PLUS Lead to (B) (Base Q4)	VOLTS (LOW) = _____ VOLTS (HIGH) = _____ TIME = _____
GROUND Lead to (C) (Collector Q4)	VOLTS (LOW) = _____ VOLTS (HIGH) = _____ TIME = _____

8. Increase the Voltage at (B) slowly (100K POT) until the output on the METER (Switch A UP) "pulses". Observe the results. The circuit is now Biased as a FREE RUNNING "ASTABLE" MULTIVIBRATOR.

Enter the observations of the Astable or Free running Multivibrator below:

Free-Running Multivibrator
ON TIME _____ ON VOLTAGE _____
OFF TIME _____ OFF VOLTAGE _____

Ed-Lab | COMPLEMENTARY MULTIVIBRATOR | EXP. NO. 7 Page No. 1

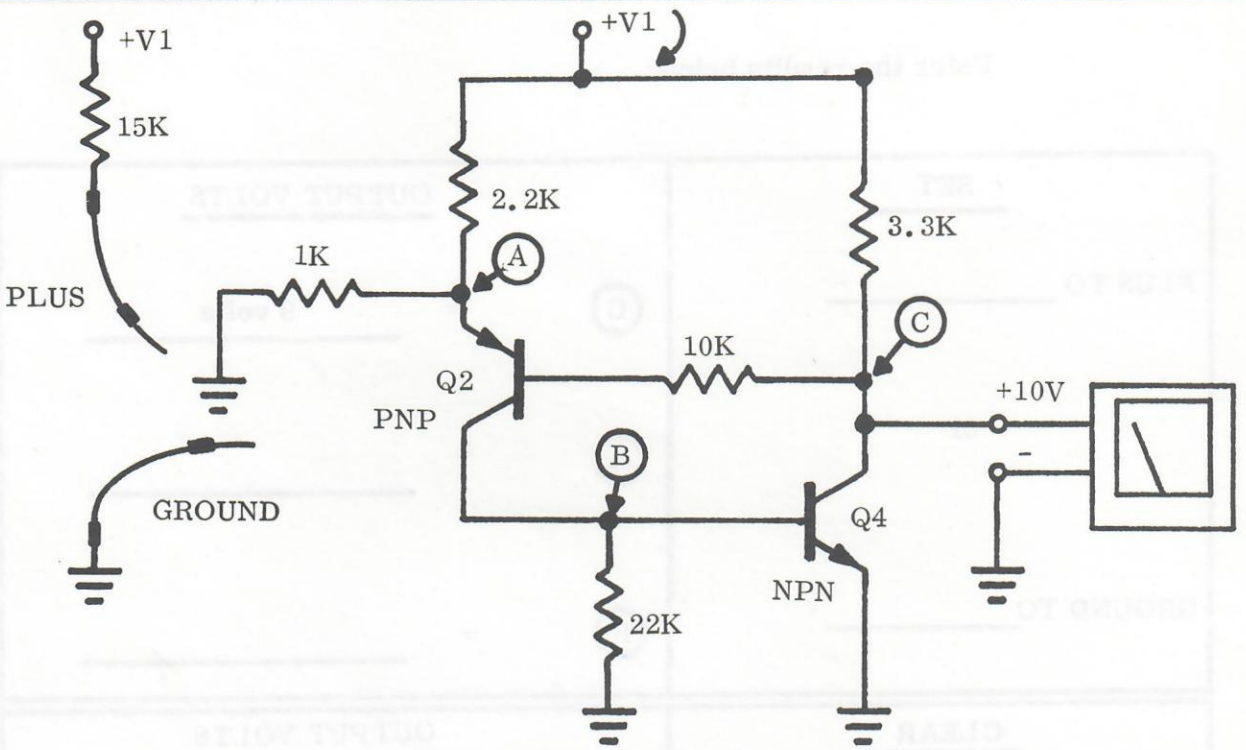


Figure 7 - 1 Complementary Bistable

Objective:

You will use complementary PNP and NPN transistors in a COMPLEMENTARY BISTABLE MULTIVIBRATOR circuit.

Description:

When transistor Q4 (NPN) is ON, the voltage at (C) is zero, which keeps transistor Q2 (PNP) ON, which in turn provides current at (B) to keep Q4 ON.

When Q4 (NPN) is OFF, +9 volts is applied to the Base of Q2 (PNP) which keeps Q2 OFF because the emitter (A) is biased at approximately +3 volts (1K and 2.2K voltage divider).

The transistors are thus both ON or both OFF in two stable conditions.

Procedure:

1. Wire the circuit in Figure 7 - 1.
2. Observe the output voltage on the meter.
3. SET and CLEAR the Flip-Flop. Determine how to Set and Clear the flip-flop by using the PLUS and GROUND wires.

Ed-Lab	COMPLEMENTARY MULTIVIBRATOR	EXP. NO. 7 Page No. 2

Enter the results below:

SET	OUTPUT VOLTS
PLUS TO _____	(C) = 9 volts
or	(A) = _____
GROUND TO _____	(B) = _____

CLEAR	OUTPUT VOLTS
PLUS TO _____	(C) = 0 volts
or	(A) = _____
GROUND TO _____	(B) = _____

Summary:

The first 7 Experiments in PULSE & WAVESHAPING & DIGITAL CIRCUITS have all been performed using a METER as the output measuring instrument and have used LOW speeds. Timing was controlled by Resistor-Capacitor Circuits. All remaining experiments in this unit use the OSCILLOSCOPE as the measuring instrument and operate at HIGH speeds.

The basic circuit configurations used in these experiments apply to all

other circuits and have included:

(a) D.C. input (Resistor) Coupled Amplifier (Inverter)
(b) A.C. input (Capacitor) Coupled (R-C) Amplifier
(c) D.C. and A.C. Coupled Amplifiers or Multivibrators:
... resulting in Bistable, Astable and Monostable Multivibrators (MV)
(d) Emitter-Coupled Multivibrators (A.C. and D.C.)
(e) Complementary Coupled Multivibrators

Resistors and Capacitors are used for timing and it is important to know which Resistors and Capacitors are used for TIMING, OR BIASING, or LOADS, or A.C. COUPLING only.

Ed-Lab	VARIABLE Frequency Pulse Generator	EXP. NO. 8 Page No. 1

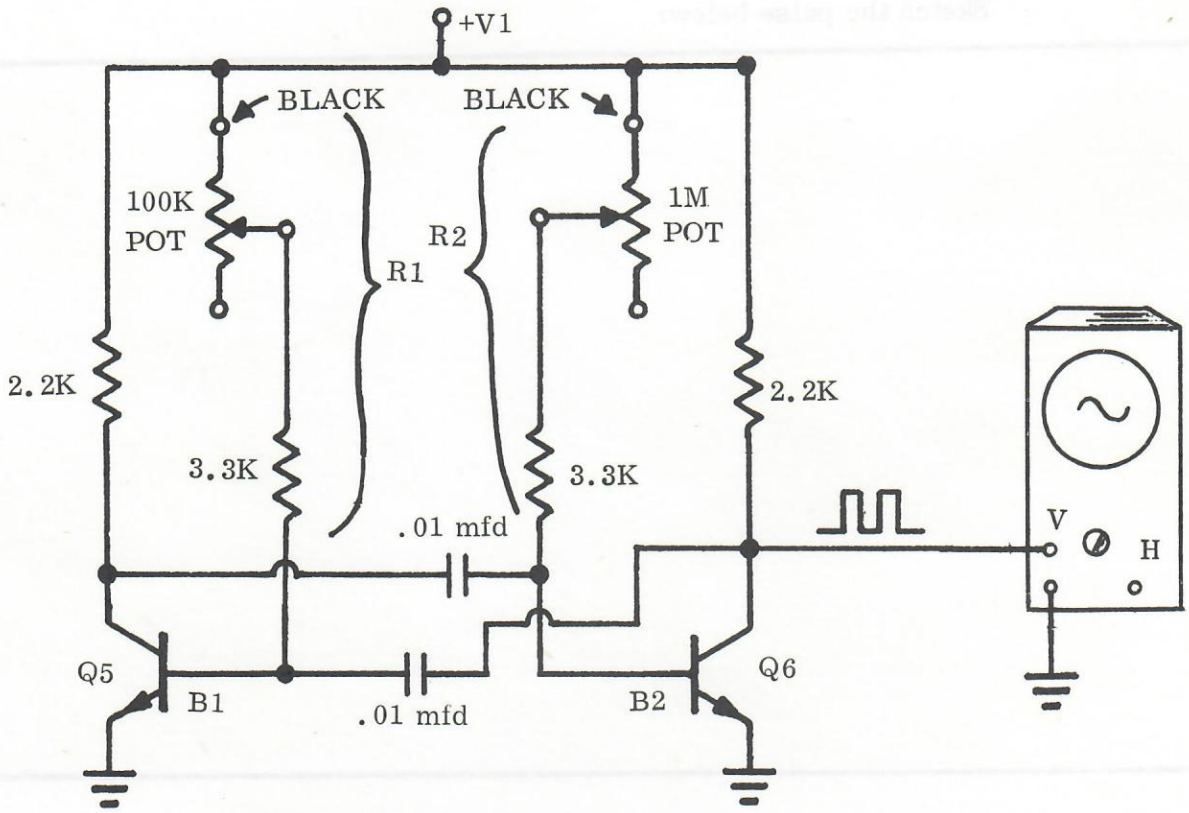


Figure 8 - 1. Variable Astable Multivibrator

Objective:

You will test an ASTABLE MULTIVIBRATOR at high frequencies and vary the frequency. You will study the effects of Base Resistors which are "too-high" and "too-low".

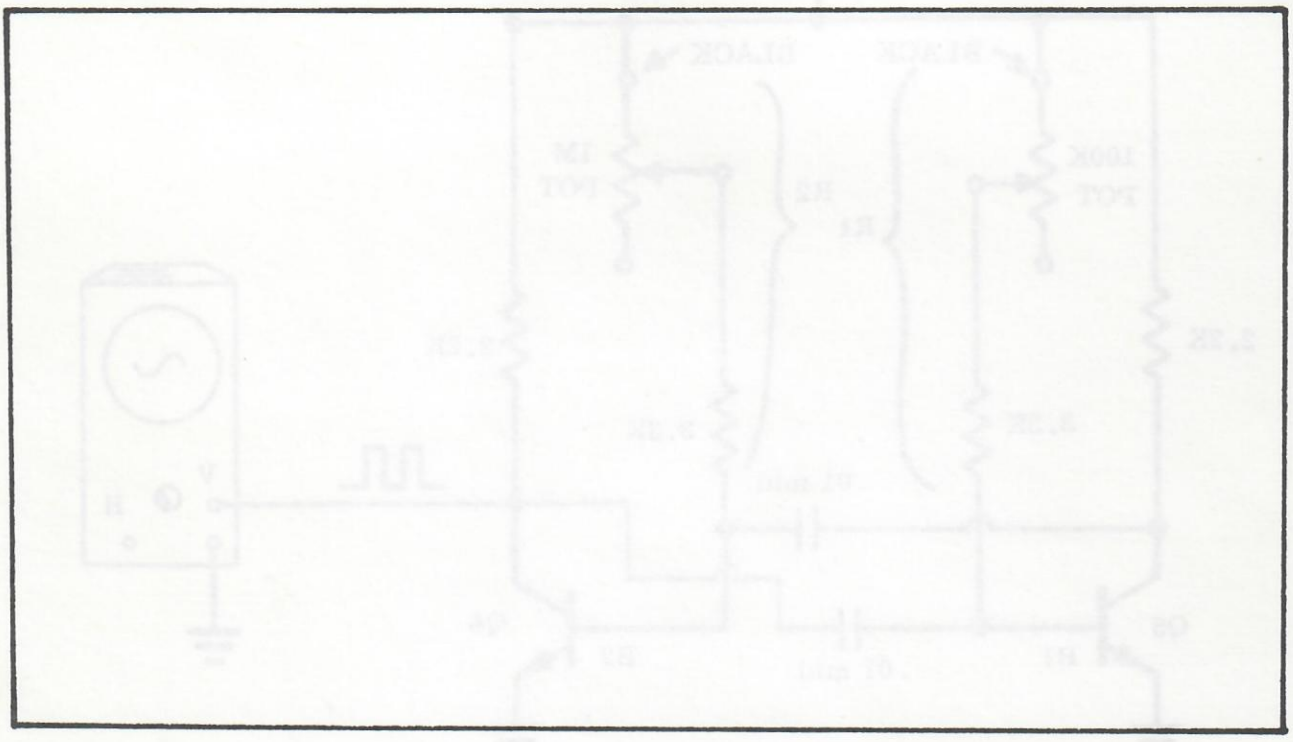
Procedure:

1. Wire the Astable Multivibrator. The 100K POT and the 1M POT are used to vary the Base Resistance and timing.

2. Set the 100K POT at a maximum of 100K and the 1M POT at approximately 100K. Measure the PERIOD (time) of a single pulse (WIDTH plus SPACING) if a Calibrated Time-Base Oscilloscope is available.

PERIOD =

Sketch the pulse below:



3. Recall the estimate for pulse width in the previous experiments as the time constant:

$$\tau = RC$$

$$\text{Approximate Period} = 2\,RC$$

$$= 2\,(100\ 10^{3})\ (.01\ 10^{-6})$$

$$= 2\,(.001)$$

$$\text{Approximate Period} = .002 \text{ seconds}$$

How does this compare with your measured period?

4. Leave the 100K POT at full. Vary the 1 MEGOHM POT. Observe that when the 1 MEG POT is at zero, the pulse is very short but the pulse does not reach full amplitude because the collector resistance is too high for the "loading" coupling capacitance.

Sketch this short pulse below: $R_1 = 103.3K$ $R_2 = 3.3K$

Sketch the waveforms at Bases B1 and B2.

B1

B2

5. Increase the MEGOHM POT and observe that the "positive pulse" widens, but as the base resistance increases (above approximately 300K), the zero level is not held at zero. The transistor is no longer "saturated" because the combination of Transistor Beta (Current Gain) and Base Resistance and Collector Resistance is not correct.

Sketch a NON-SATURATED waveform below (where the zero is not held at zero volts; 1 meg POT at approximately 500K)

UNSATURATED SIGNAL

Full saturation occurs when

(Collector Current, I_c) = (Beta)(Base Current I_B)

Where both collector and base resistors are connected to the same voltage (as in the Astable);

$$I_C = \frac{V}{R_B}$$

$$I_B = \frac{V}{R_B}$$

$$I_C = \beta I_B$$

$$\frac{V}{R_C} = \beta \frac{V}{R_B}$$

FOR SATURATION $\frac{R_B}{R_C} = \beta$

If saturation does not occur in a circuit, reduce R_B, or increase R_C, or use a higher Beta transistor.

6. First Set R_1 (100K) pot to zero.
Set R_2 (1M) pot to maximum (1M).

The Astable will probably not operate.
(If the Astable does operate, momentarily connect one collector to GROUND and the Astable should start.)

If the transistors are held "too much ON", the Astable will not START.

7. Start the astable by momentarily removing (then replacing) ANY lead.

Stop it by grounding any collector; and then start it by removing and then replacing any lead.

8. Adjust the Astable to the highest frequency. The 100K POT and 1M POT are both set to zero.

Sketch the waveform below and measure the PERIOD

Calculate the FREQUENCY

Maximum FREQUENCY =

9. Adjust both POTS to obtain the lowest frequency. What is the lowest frequency?

PERIOD =

LOWEST FREQUENCY =

Ed-Lab | VARIABLE Duty Cycle and Rise Time | EXP. NO. 9 Page No. 1

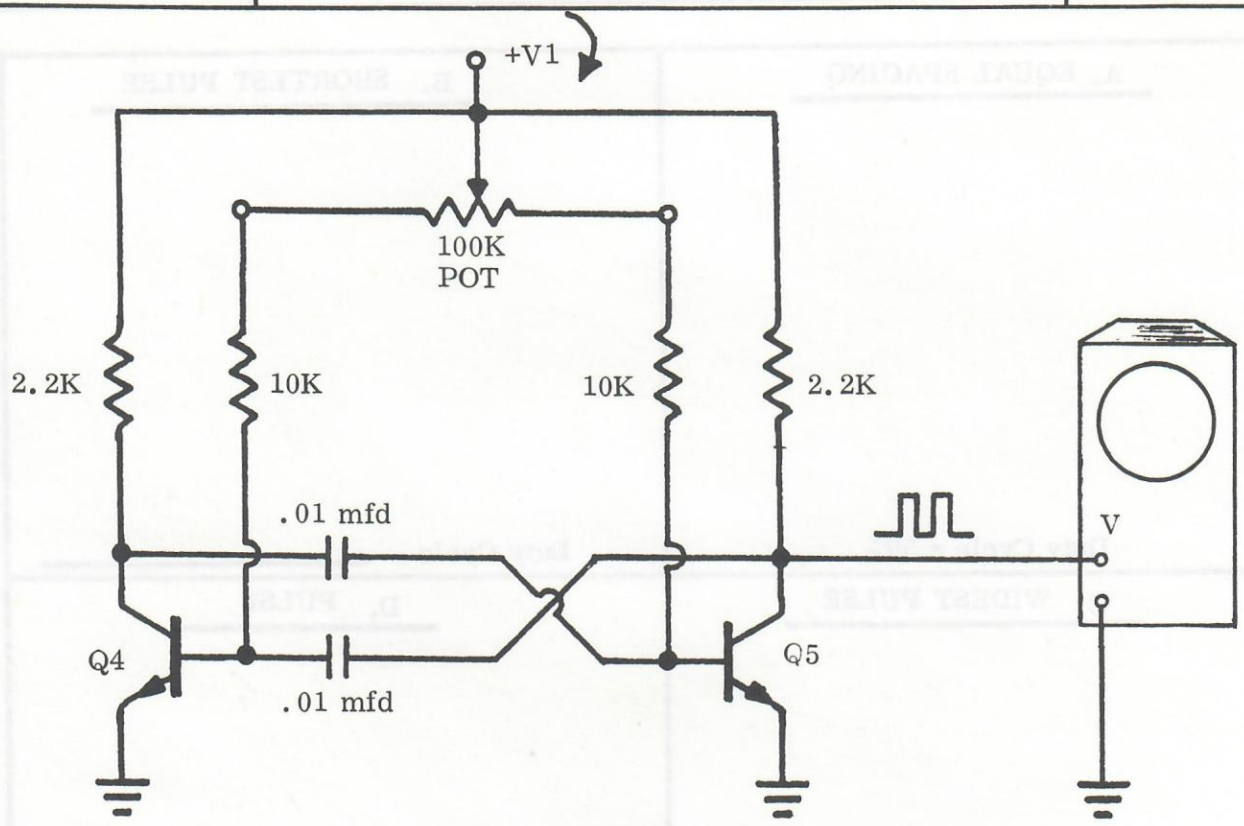


Figure 9-1 Variable Duty Cycle Astable

Objective:

You will vary the Base Resistors in an Astable Multivibrator to result in a variable Pulse Width and variable Duty Cycle. You will add an ISOLATION DIODE to reduce the rise-time.

Procedure:

1. Wire the circuit in Figure 9-1. Varying the 100K POT results in shifting the 100K POT Resistance continuously between the two base resistors.

2. Observe the output variation in pulse width and spacing as the Potentiometer is varied. Sketch waveforms below for various "duty cycles". The duty cycle is the Ratio between the ON pulse and the FULL PERIOD.

$$\text{DUTY CYCLE} = \frac{\text{PULSE "ON" TIME}}{\text{FULL PULSE PERIOD}}$$

A. EQUAL SPACING	B. SHORTEST PULSE
Duty Cycle = 50%	Duty Cycle - _____
C. WIDEST PULSE	D. PULSE
Duty Cycle = _____	Duty Cycle = 25% Rise Time = _____ Fall Time = _____

3. Measure the rise time and fall time for the pulse sketched in "D" above.

PULSE RISE TIME =
PULSE FALL TIME =

Observe that the FALL TIME is difficult to measure and can be considered as close to zero. The rise time is a result of the collector resistor and load which is the coupling capacitance. Rise time can be reduced a little by decreasing the collector resistor. Decreasing the coupling capacitor cannot be done because it determines the oscillation frequency. A DECOUPLING DIODE (D) is used with a Resistor (R) as shown in the figure below. The

output voltage rises quickly and "back-biases" the diode which "decouples" the capacitor from the collector resistor. The added R (3.3K) recharges the coupling capacitor.

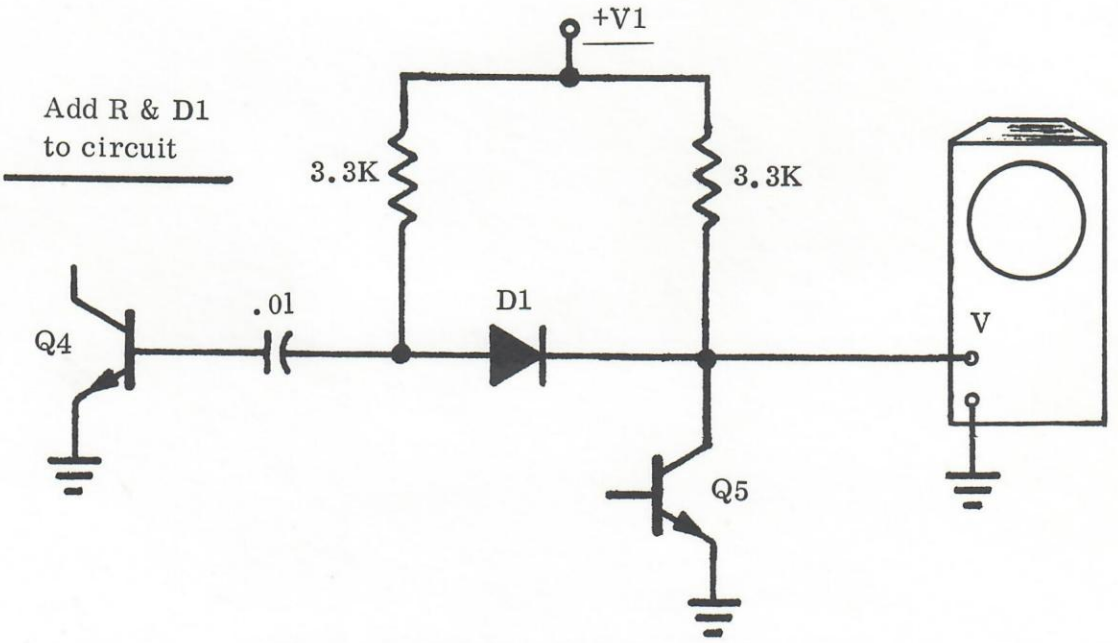


Figure 9-2 Decoupling Network

4. Wire the changes in the circuit by adding the R (3.3K) and D1 as shown in Figure 9-2.

5. Observe the output waveform. Sketch the waveform below and estimate the new RISE TIME (if possible):

How does the Rise Time compare with the previous Rise Time without the Decoupling Network?

Ed-Lab	COMPLEMENTARY ASTABLE	EXP. NO. 10 Page No. 1

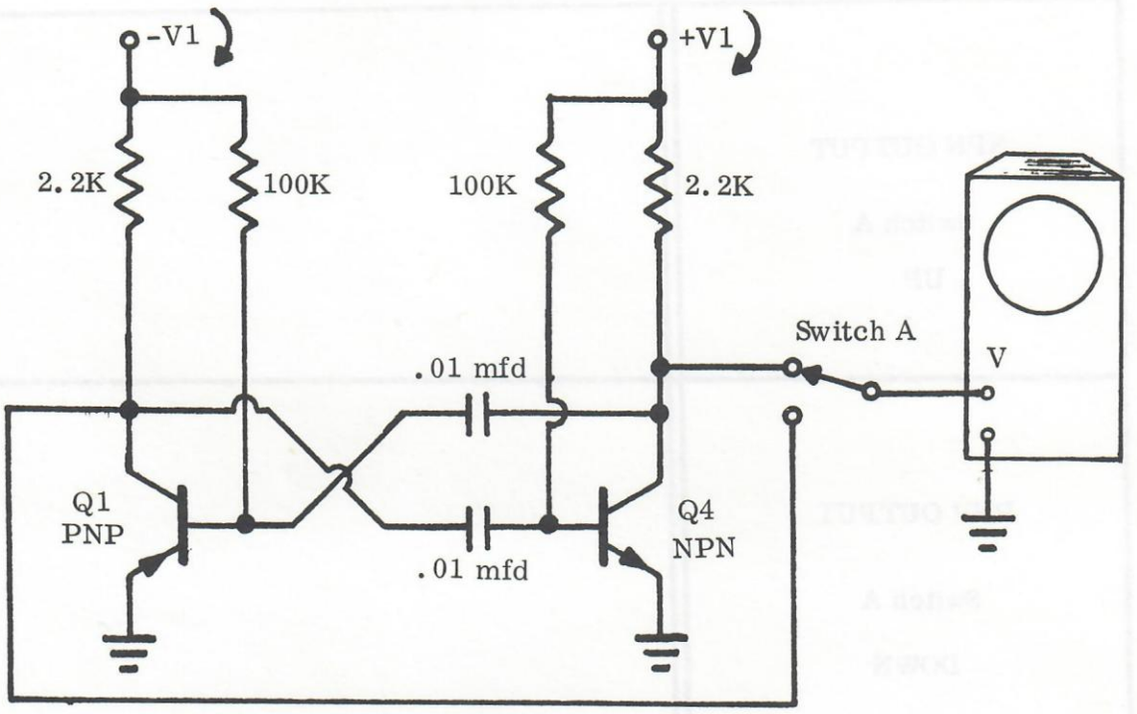


Figure 10 - 1 Complementary Astable

Objective:

You will use a "Complementary Pair" NPN and a PNP transistor with "Coupling Capacitors" in a Complementary Astable Multivibrator circuit.

Procedure:

1. Wire the Circuit in Figure 10 - 1.

   This circuit is similar to the standard ASTABLE MULTIVIBRATOR except that with the Complementary pair, the transistors are both ON or both OFF. Because the OFF time is controlled by the time constant RC and the ON switching is fast. the ON time is very short and the transistors are both OFF most of the time. The result is a low power circuit. The smallest time constant should control the PERIOD.

2. Observe the outputs on the oscilloscope. Sketch both outputs on the following page. (Indicate the D.C. Voltage Levels)

NPN OUTPUT Switch A UP	
PNP OUTPUT Switch A DOWN	

3. Measure the PERIOD on the Oscilloscope.

PERIOD =

4. How does the time constant correspond to the period?

$$\tau = RC$$
$$= (100\ 10^{3})\ (.01\ 10^{-6})$$
$$= 10^{-3}$$
$$\tau = 1 \text{ milliseconds}$$
(or 1,000 micrseconds)

Ed-Lab	COMPLEMENTARY ASTABLE	EXP. NO. 10 Page No. 3

5. Calculate the frequency from the measurement in (3) above

FREQUENCY =

6. Measure the PULSE WIDTH.

PULSE WIDTH =

7. The Period should be controlled by only the Shortest Time Constant. Change any one capacitor to 0.25 mfd. Does the period change?

8. Change the capacitor back to 0.01 mfd and change the other capacitor to .25 mfd. Does the Period change?

9. Change both capacitors to 0.25 mfd. Does the Period change? What are the Period and Frequency?

PERIOD (C = 0.25 mfd) =

FREQUENCY (C = .25 mfd) =

Ed-Lab | EMITTER COUPLED ASTABLE | EXP. NO. 11 Page No. 1

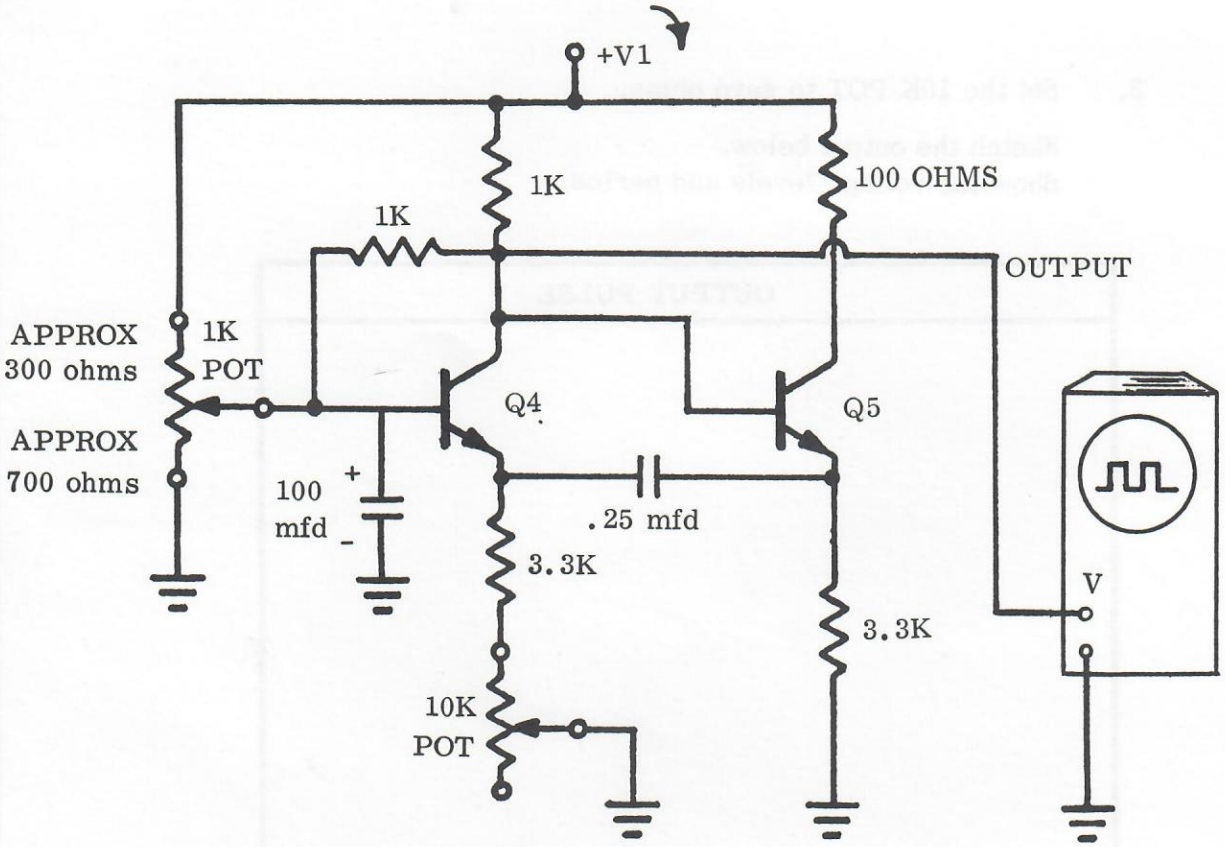


Figure 11 - 1 Emitter Coupled Astable

Objective:

You will build and test an EMITTER COUPLED ASTABLE MULTIVIBRATOR.

Procedure:

1. Wire the Circuit in Figure 11 - 1.

   The Transistor Q4 output (collector) is directly connected to the Transistor Q5 input (base). The two emitters are coupled by the 0.25 mfd Capacitor.

2. Observe the output on the Oscilloscope. Adjust the bias 1K POT for a pulse output.

3. Set the 10K POT to zero ohms.

   Sketch the output below.
   Show the voltage levels and period.

OUTPUT PULSE

4. Vary the 10K POT and observe the results. Sketch the waveform below for a full POT setting of 10K.

OUTPUT PULSE

Ed-Lab | VARIABLE MONOSTABLE MULTIVIBRATOR | EXP. NO. 12 Page No. 1

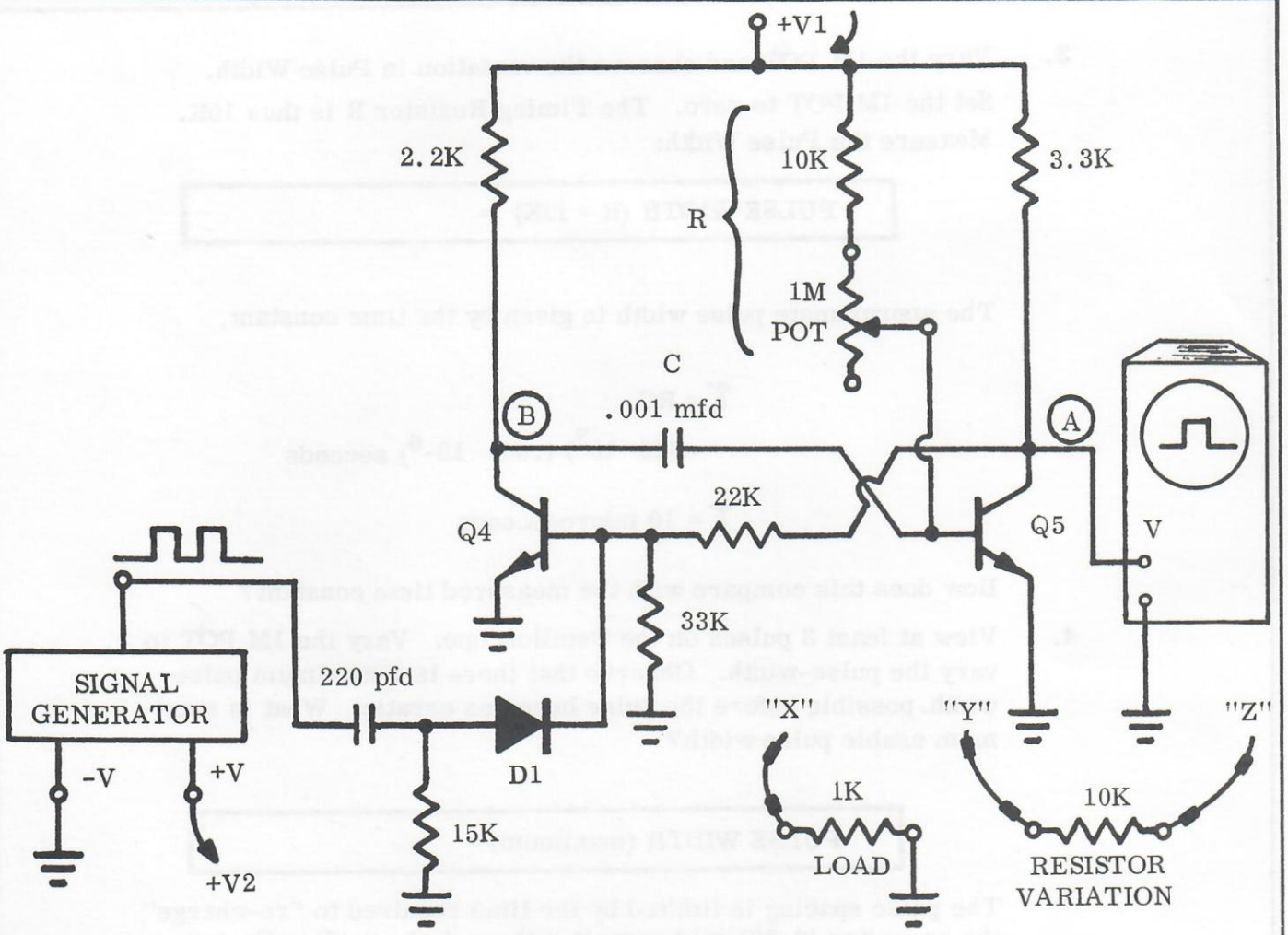


Figure 12 - 1 MONO

Objective:

You will use a small RC Time Constant with a Trigger input and test a VARIABLE PULSE WIDTH MONOSTABLE MULTIVIBRATOR.

Description:

The Monostable Multivibrator circuit in Figure 12 - 1 is the standard circuit from Experiment No. 5. An input Trigger is provided from the Ed-Lab SIGNAL GENERATOR Square Wave to the base of Q4. The Square Wave is "differentiated" (220 pfd and 15K) to provide a short trigger pulse. Diode D1 enables only the POSITIVE TRIGGER to operate. The effect of not using D1 will be demonstrated. The 1M POT Resistance controls the Pulse Width.

Procedure:

1. Wire the circuit in Figure 12 - 1.
2. The Ed-Lab Signal Generator Power Supply voltage terminals must be connected. Be sure to connect the +V terminal to the +V2 voltage; and the -V terminal to GROUND.

3. Vary the 1M POT and observe the variation in Pulse Width.

Set the 1M POT to zero. The Timing Resistor R is thus 10K. Measure the Pulse Width:

PULSE WIDTH (R = 10K) =

The approximate pulse width is given by the time constant,

$$\tau = RC$$

$$= (10 \quad 10^{3}) \; (.001 \quad 10\text{-}^{6}) \text{ seconds}$$

$$\tau = 10 \text{ microseconds}$$

How does this compare with the measured time constant?

4. View at least 3 pulses on the Oscilloscope. Vary the 1M POT to vary the pulse-width. Observe that there is a maximum pulse-width. possible before the pulse becomes erratic. What is maximum usable pulse width?

PULSE WIDTH (maximum) =

The pulse spacing is limited by the time required to "re-charge" the capacitor (0.001 mfd capacitor through the 2.2K collector resistor). What is the maximum duty cycle?

DUTY CYCLE (maximum) =

5. The pulse width is determined by R (10K + 1M Pot) and C (.001 mfd). Test the effect of "loading and varying the circuit component values. Set the 1M POT to zero. Connect Lead "X" with a 1K LOAD to the collectors at point A , and then at point B . What is the effect of loading on the two outputs?

Ed-Lab	VARIABLE MONOSTABLE MULTIVIBRATOR	EXP. NO. 12 Page No. 3

LOADING	EFFECT
A 1K TO GROUND	WIDTH_____ AMPLITUDE_____
B 1K to GROUND	WIDTH_____ AMPLITUDE_____

Connect the 10K Resistor (leads Y and Z) across the circuit resistors to determine the effect of "PARAMETER VARIATION" on circuit operation.

PARAMETER VARIATION 10K Across (Leads Y & Z)	EFFECT ON Pulse Amplitude & Pulse Width
2. 2K Collector Resistor	
3. 3K Collector Resistor	
22K Coupling Resistor	
33K Bias Resistor	
10K Timing Resistor	
15K Differentiator Resistor	

6. The Diode D1 is used to pass or transmit only the Positive Pulse. Short-Circuit the Diode, D1 (i.e., use a direct wire without the diode).

   Vary the 1M POT. Observe that the NEGATIVE trigger pulse stops the pulse and prevents pulse-widths greater than half of the period. What is the maximum pulse width? What is the maximum duty cycle?

Ed-Lab | TRANSISTOR SWITCH BIASING | EXP. NO. 13 Page No. 1

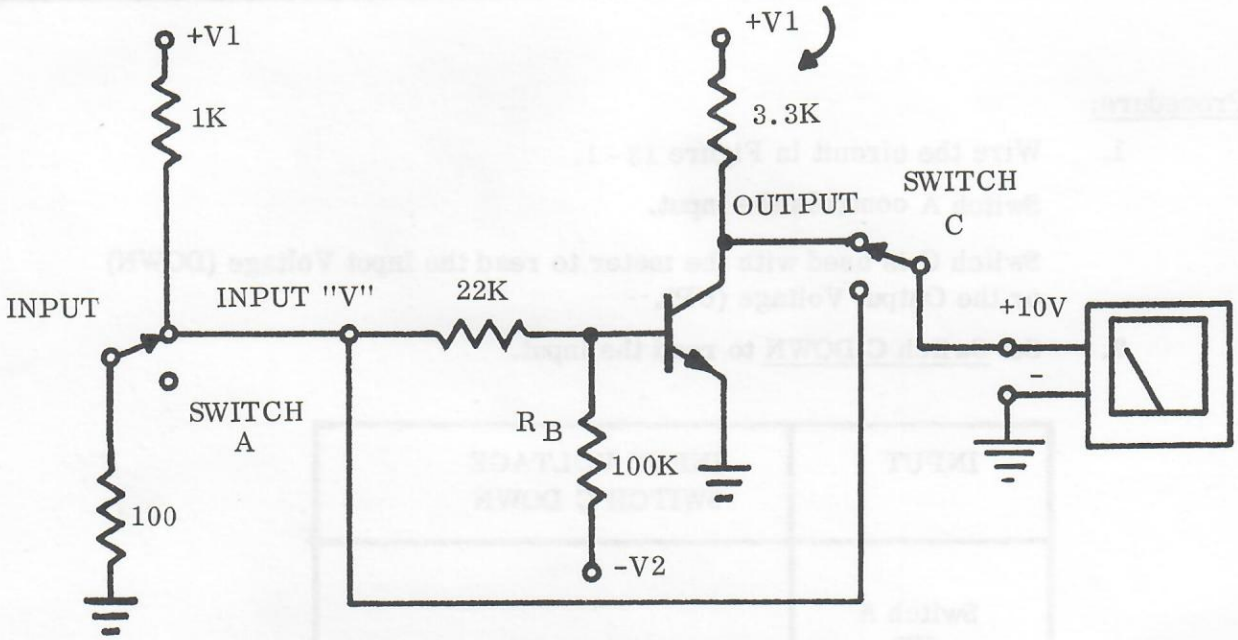


Figure 13 - 1 Transistor OFF Biasing

Objective:

You will apply a "zero - offset" input to a Transistor Switch and use a BIAS RESISTOR to obtain Transistor CUT-OFF.

Description:

In the previous experiments, a positive voltage and current were applied to the base through a base input resistor to provide base current and to put the Transistor Switch "ON" (closed-switch) resulting in an output of Zero Volts. When the input voltage, V, is zero, there is no base current; but the input "zero" voltage always has an "offset" which is higher than zero volts because of the small ON "saturation voltage" of the transistor from which the input is obtained or from some "noise" voltage.

Switch A is used for the input, but a 100 ohm resistor is connected to ground to simulate a transistor on-resistance. The zero voltage will thus be offset due to the voltage divider between the 1K and 100 ohm resistors. This voltage would then be "offset" to approximately 1 volt rather than zero volts. The 1 volt input will result in the transistor being ON rather than OFF.

It will be necessary to provide a bias resistor, R_B, connected to a negative voltage to obtain a cutoff bias. Germanium transistors usually have bias resistors in circuits such as the Inverter, Bistable Multivibrator, and Monostable Multivibrator.

Procedure:

1. Wire the circuit in Figure 13 - 1.

   Switch A controls the Input.

   Switch C is used with the meter to read the Input Voltage (DOWN) or the Output Voltage (UP).

2. Set Switch C DOWN to read the input.

INPUT	INPUT VOLTAGE SWITCH C DOWN
Switch A UP (zero offset)	
Switch A DOWN	

3. Set Switch C UP to read the output voltage. Operate the input and record the output in column A below:

	INPUT	OUTPUT With R_B 100K (A)	OUTPUT Without R_B (B)	OUTPUT Silicon Q7 Without R_B (C)	OUTPUT Silicon Q7 With R_B (D)
Switch A UP zero offset					
Switch A DOWN					

4. Remove the resistor (R_B = 100K) from the circuit by disconnecting the lead connected to -V2 and repeat the above test and enter the data in column B above. Does the circuit operate properly without R_B?

5. Leave R_B removed from the circuit. Substitute the Silicon Transistor, Q7, for the Germanium Transistor and repeat the test entering the data in column C in the table. How do the results compare with the other tests?

6. Leave the Silicon Transistor in the circuit and connect R_B back to -V2 in the circuit. Repeat the test and enter the data in Column D Comment on the results.

7. Inverters with NPN Transistors use Positive Collector Voltages. Circuits using PNP Transistors use Negative Collector Voltages. When NPN circuits are used to drive PNP circuits a "voltage inversion" circuit is used with a "reversed bias" voltage. The circuits are shown below for "Negative to Positive" and "Positive to Negative" Voltage Inversions.

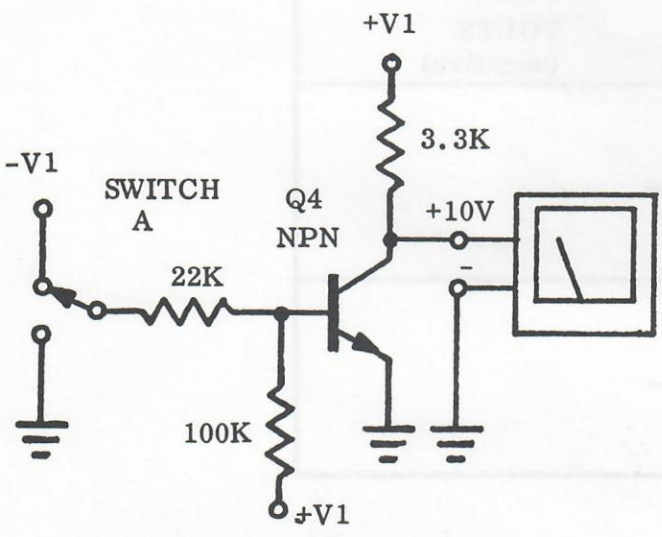


Figure 13 - 2
Negative to Positive Inversion

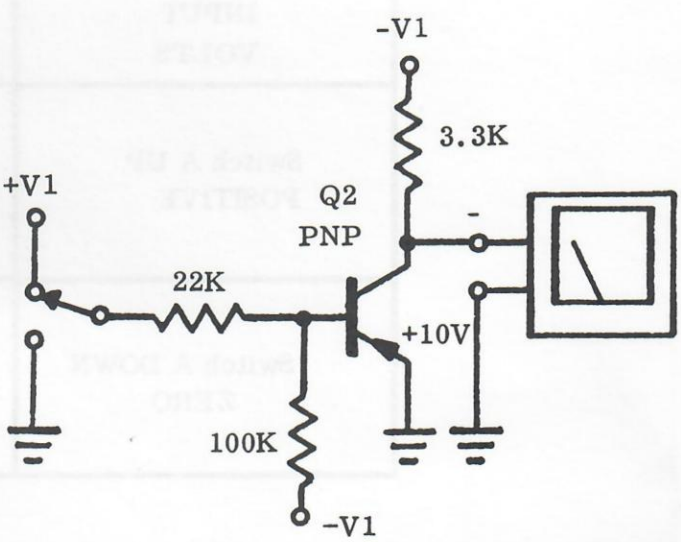


Figure 13 - 3
Positive to Negative Inversion

8. Wire the circuit in Figure 13 - 2.

9. Operate the input (Switch A) and enter the results below:

INPUT VOLTS	OUTPUT VOLTS
Switch A UP NEGATIVE	+
Switch A DOWN ZERO	+

10. Wire the circuit in Figure 13 - 3.

11. Enter the results of the test in the table below:

INPUT VOLTS	OUTPUT VOLTS (negative)
Switch A UP POSITIVE	−
Switch A DOWN ZERO	−

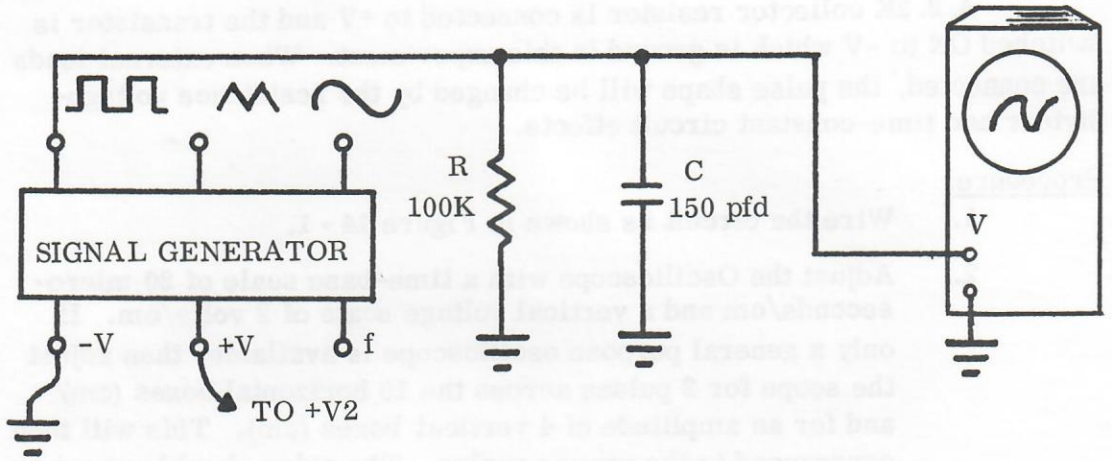


Figure 14 - 1 R-C Loading

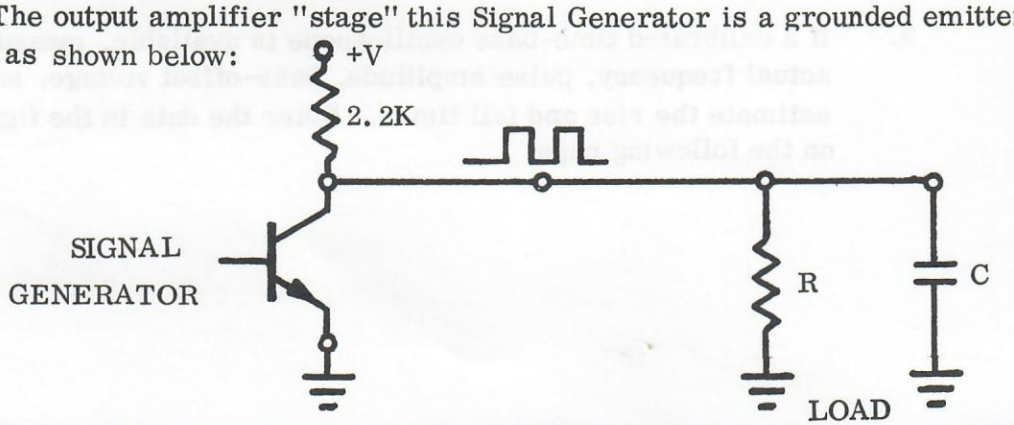
Objective:

You will use the internal SIGNAL GENERATOR and observe the SQUARE WAVE PULSE output under various Resistive and Capacitive Loads.

Description:

The internal Signal Generator has three outputs; a SQUARE WAVE, TRIANGULAR WAVE and SINEWAVE. Power must be connected to this Signal Generator. The (+V) terminal is connected to +V2 (10 volts) and the (-V) terminal is connected to GROUND in this experiment. The pulse operates at an approximate frequency of 10,000 hertz or 10,000 pps (pulses per second) and with an amplitude of approximately 8 volts. The input terminal (f) varies the frequency but is not used in these experiments.

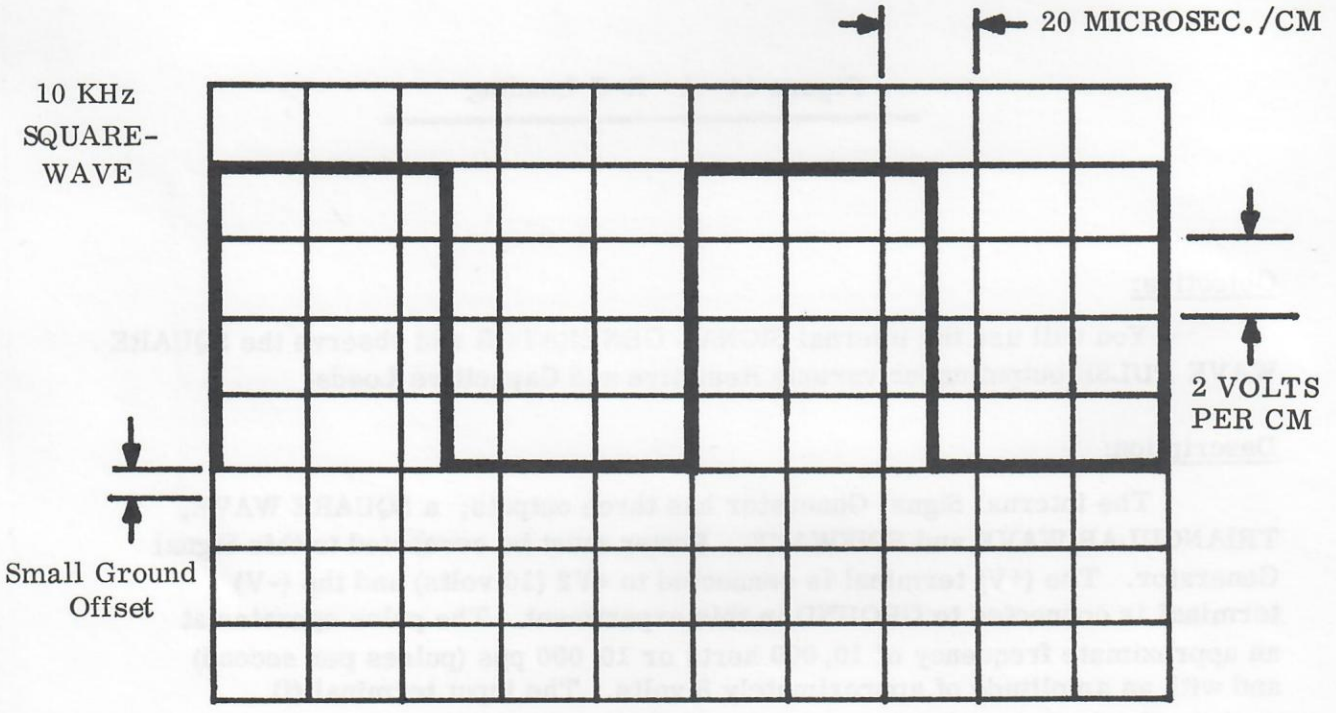
The output amplifier "stage" this Signal Generator is a grounded emitter amplifier as shown below:



A 2.2K collector resistor is connected to +V and the transistor is switched ON to -V which is ground in this experiment. When external loads are connected, the pulse shape will be changed by the resistance voltage-divider and time-constant circuit effects.

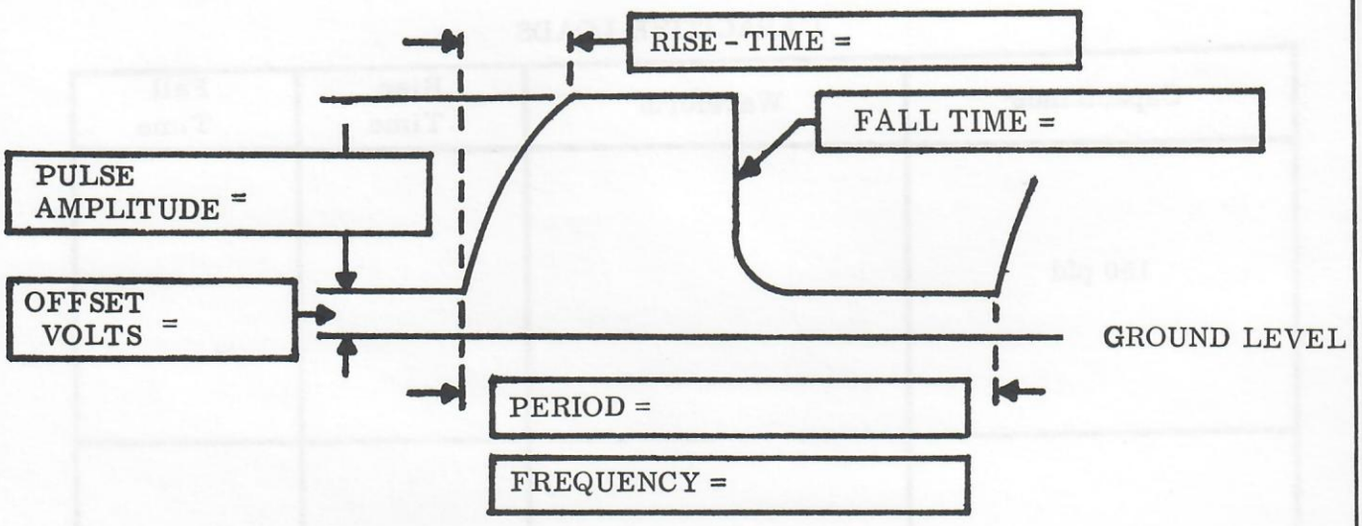
Procedure:

1. Wire the circuit as shown in Figure 14 - 1.
2. Adjust the Oscilloscope with a time-base scale of 20 micro-seconds/cm and a vertical voltage scale of 2 volts/cm. If only a general purpose oscilloscope is available, then adjust the scope for 2 pulses across the 10 horizontal boxes (cm) and for an amplitude of 4 vertical boxes (cm). This will then correspond to the proper scales. The pulse should appear as shown below:



'SCOPE PRESENTATION

3. If a calibrated time-base oscilloscope is available, measure the actual frequency, pulse amplitude, base-offset voltage, and estimate the rise and fall times. Enter the data in the figure on the following page:



4. Substitute various other load resistors, measure the amplitude and enter the data in the table below:

RESISTIVE LOADS

LOAD RESISTOR (R)	PULSE AMPLITUDE
100K	
10K	
2.2K	
1K	
100 ohms	

The amplitude should be half or 4 volts when the 2.2K load is used because it is equal to the collector resistance (voltage-divider equations.)

5. Remove the load resistance and substitute the capacitive loads. Sketch the waveforms below and estimate the rise-times and fall-times. Note that the rise-time is longer because the 2.2K collector load resistor is connected to the plus-volts while the fall-time is to ground through the transistor resistance of only a couple of hundred ohms.

Ed-Lab | PULSE CIRCUIT LOADING | EXP. NO. 14 Page No. 4

CAPACITIVE LOADS

Capacitance	Waveform	Rise Time	Fall Time
150 pfd			
.001 mfd			
.01 mfd			
.25 mfd			
(Capacitance between your two hands.)			

What do you estimate is the capacitance and resistance between your hands (by observing the drop in amplitude and the rise time)?

5. Later experiments will demonstrate Pulse Driver Circuits that are used to reduce the effects of LOADS. These include the EMITTER FOLLOWER, COMPLEMENTARY EMITTER FOLLOWER, FEEDBACK AMPLIFIER, and CASCODE or TOTEM-POLE AMPLIFIER, and CASCODE COMPLEMENTARY AMPLIFIER.

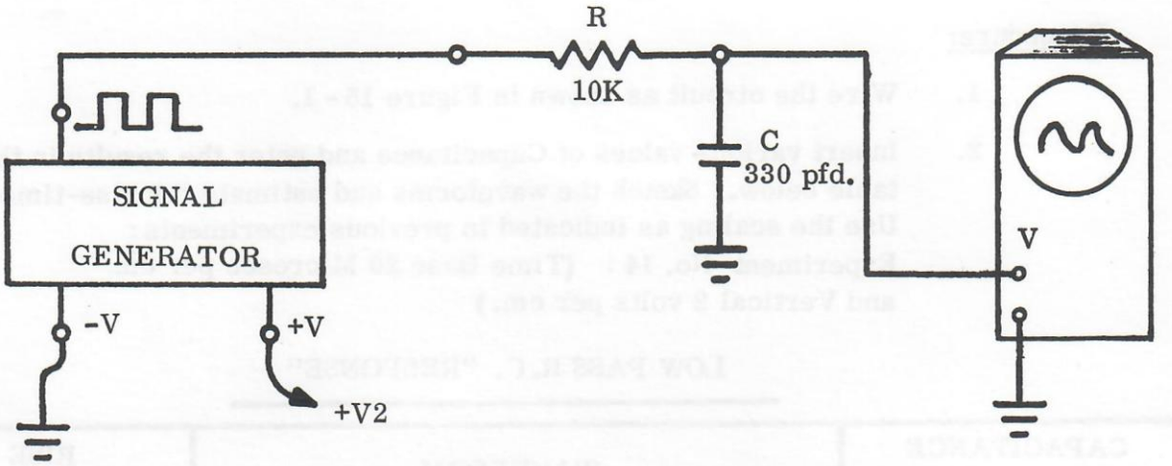


Figure 15-1 Low Pass R.C. Circuit

Objective:

You will use a LOW PASS Resistor-Capacitor Circuit and observe and measure the effect on a pulse waveform.

Description:

The Low-Pass circuit or "network" transmits low frequency signals and attenuates or reduces the amplitude of high frequency signals as studied in the A.C. Circuit Theory units. The effect on a pulse is to increase the rise-time and increase the fall time.

Circuits of this type using resistors, capacitors and inductors are referred to as PASSIVE WAVESHAPING circuits. When transistors are used, the circuits are called ACTIVE WAVESHAPING circuits. In some applications, the R and C Low Pass elements are used to SHAPE the pulse. In other cases, the R and C elements are in other parts of the circuit and affect the rise and fall time in an undesired way. We must then use circuits to reduce the effect of these STRAY elements and LOAD elements.

Ed-Lab	LOW PASS R. C. CIRCUIT	EXP. NO. 15 Page No. 2

Procedure:

1. Wire the circuit as shown in Figure 15 - 1.
2. Insert various values of Capacitance and enter the results in the table below. Sketch the waveforms and estimate the rise-time. Use the scaling as indicated in previous experiments: Experiment No. 14 : (Time Base 20 Microsec per cm and Vertical 2 volts per cm.)

LOW PASS R.C. "RESPONSE"

CAPACITANCE for R = 10K)	WAVEFORM	RISE TIME
330 pfd		
001 mfd		
.01 mfd		*(measure rate in volts per second.)
.25 mfd	(change scale on oscilloscope)	

*There is no rise-time, but a sweep voltage.

3. Which signal would you use to generate a "linear voltage sweep circuit"?

A linear voltage sweep circuit would typically be used to control the "horizontal sweep" on an oscilloscope. There is really no rise-time on the linear sweep because the R and C are so large that the pulse never reaches full voltage. This circuit is also an INTEGRATOR. What is the RATE in volts per second for the 0.01 mfd capacitor circuit.

RATE =	volts per second*

* or in "volts per millisecond".

The theoretical response in an R.C. circuit is an EXPONENTIAL given by:

$$e^{-t/RC}$$

The rising signal is given by:

$$V(t) = Vm\,(1 - e^{-t/RC}$$

The falling signal is given by:

$$V(t) = V_m\, e^{-t/RC}$$

The theoretical RATE for the starting or linear portion of the waveform is:

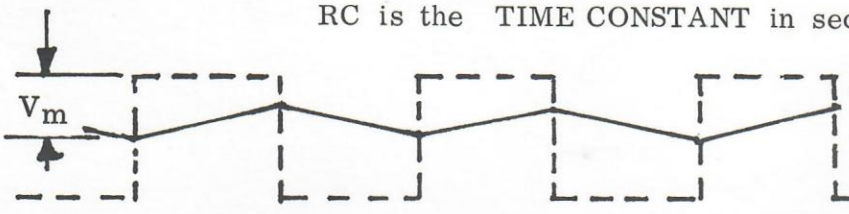
$$\text{RATE} = \frac{V_m}{RC}$$

where: R is in ohms

C is in farads

V_m is in volts, and is the charging voltage

RC is the TIME CONSTANT in seconds



The square wave amplitude is 8 volts and V_m is 4 volts.

The theoretical rate approximation is:

$$\text{RATE} = \frac{V_m}{RC} \frac{4}{(10K)(0.01\ 10^{-6})}$$

RATE = 40,000 VOLTS PER SECOND

TIME CONSTANT (τ) = RC = _____

How does this compare with your measurements? There will be differences due to inaccuracies in reading on the oscilloscope, tolerances of the components, other circuit capacitances or resistances, and because the rate is only valid at the start of the exponential your measurement should show a lower rate.

Ed-Lab	HIGH PASS R. C. CIRCUIT	EXP. NO. 16 Page No. 1

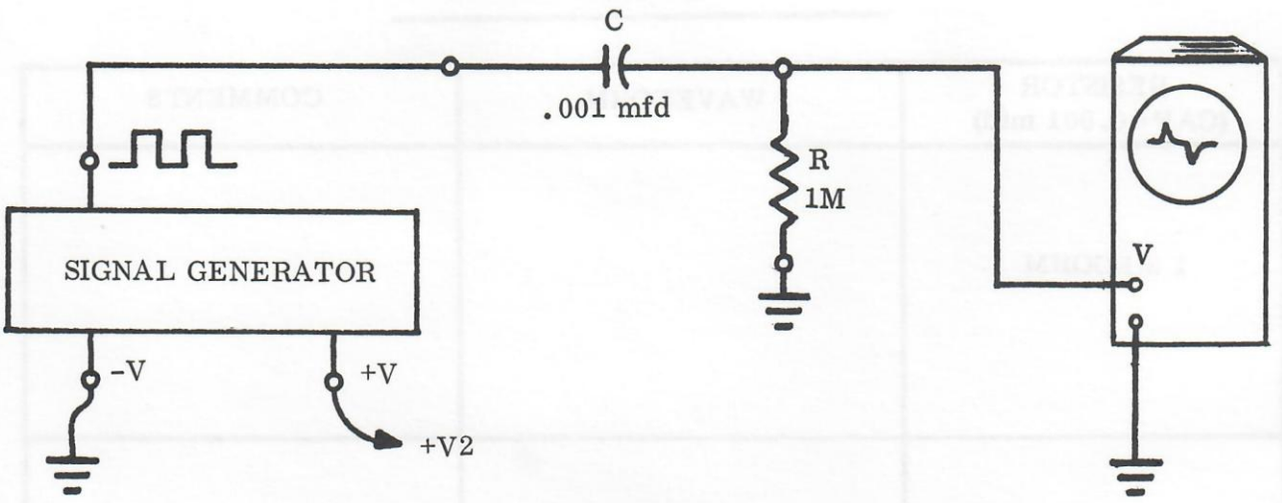


Figure 16 - 1 High Pass R.C. Circuit

Objective:

You will observe the output from a High Pass R.C. Circuit using various Time Constants. You will use the R.C. Network and a Diode to generate sharp pulses.

Description:

The above R.C. network is a High Frequency Pass circuit. The circuit also changes the D.C. LEVEL and the pulse develops a "Droop". This type of circuit is used to change the pulse level and to "shorten" a pulse.

Pulses can also be used to measure the FREQUENCY RESPONSE of an amplifier. The Rise Time indicates the high frequency response, and the pulse "droop" indicates the low frequency response.

Procedure:

1. Wire the circuit in figure 16 - 1.
2. Sketch the output waveforms using the various time constants (R C) given and enter the results in the chart below. Be sure to show the GROUND or ZERO VOLTAGE level.

R C HIGH PASS CIRCUIT

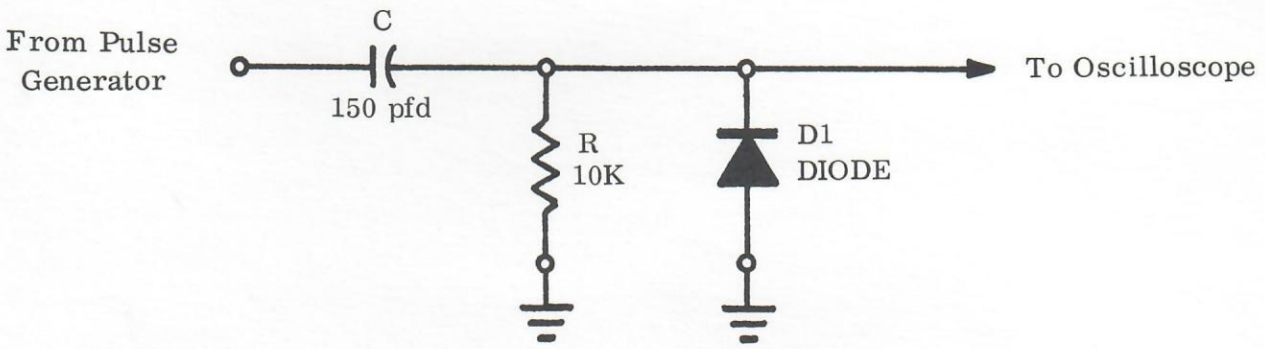
RESISTOR (CAP = 0.001 mfd)	WAVEFORM	COMMENTS
1 MEGOHM		
100K		
10K		
2.2K		
R = 2.2K Use the capacitance between your hands.		

Observe that the positive "pulse amplitude" using the 2.2K resistor is half of the negative pulse amplitude. This is due to the voltage-divider load to the 2.2K collector resistor.

3. Measure the pulse top DROOP in volts using the oscilloscope for the circuit using the 100K resistor.

DROOP = _____VOLTS

4. Substitute the following Capacitor, Resistor and Diode in the High Pass Circuit.



The diode in the above circuit will "CLIP" off the negative pulse.

5. Sketch the waveforms with the diode in both directions and without the diode.

WAVEFORMS

Circuit Above	No Diode	Reversed Diode

Ed-Lab	HIGH PASS R. C. CIRCUIT	EXP. NO. 16 Page No. 4

The High Pass R.C. Circuit is a DIFFERENTIATOR and is used to generate short pulses or SPIKES and is frequently called a PULSE COMPRESSOR.

Ed-Lab	LOW PASS R. L. NETWORK	EXP. NO. 17 Page No. 1

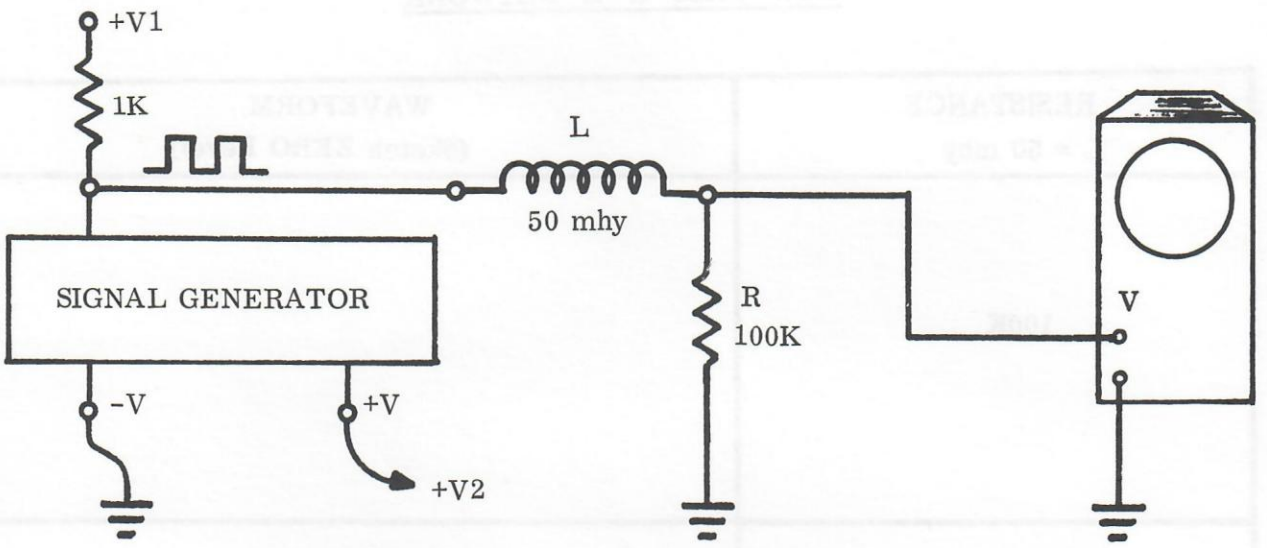


Figure 17 - 1 Low Pass R. L. Circuit

Objective:

You will observe the operation of a Low Pass Resistor - Inductor Network.

Description:

This circuit is a low frequency pass filter and operates in a manner almost identical to the low pass R. C. circuit. The time constant is:

$$\text{TIME CONSTANT} = \tau = \frac{L}{R}$$

A 1 KILOHM resistor is connected to the output of the Signal Generator to reduce the output collector resistor (2. 2K) with the parallel 1K resistor to approximately 680 OHMS.

Procedure:

1. Wire the circuit in Figure 17 - 1.
2. Observe the output on the oscilloscope. Adjust the oscilloscope as before with 2 volts per cm and 20 microseconds per centimeter. If a general purpose scope is used, adjust the scope for an amplitude with the pulse corresponding to 4 vertical boxes (centimeters) and with 2 complete pulses across the 10 horizontal boxes.
3. Substitute various resistors and sketch the outputs in the chart.

LOW PASS R-L NETWORK

RESISTANCE L = 50 mhy	WAVEFORM (Sketch ZERO Level)
100K	
10K	
1K	
100 OHMS	(Expand Vertical Scale)

This circuit can be used to provide a linear rising current in a coil such as in the CRT Picture Tube Deflection or Sweep Coil in a Television Set.

Which size resistance would you select to provide a linear sweep?

4. Substitute an R = 500 OHMS by using the 1K POT at "Half-Way". Sketch the waveform below and measure the time-base (ΔT) and amplitude (ΔV).

WAVEFORM (R = 500 OHMS) (L = 50 mhy)

5. Calculate the maximum current (ΔI). Note that the voltage is measured across the 500 ohm resistors so that:

$$\Delta I = \frac{\Delta V}{500}$$

ΔI = milliamperes

6. Calculate the current RATE in amperes per second, or milliamperes per micrsecond, or in any other similar dimensions:

$$\text{CURRENT RATE} = \frac{\Delta I}{\Delta T}$$

CURRENT RATE =

7. Calculate the TIME CONSTANT for the above circuit:

$L = 50$ millihenries $= 50 \times 10^{-3}$

$R = 500$ OHMs

$$\tau = \frac{L}{R}$$

$\tau =$

Note that the Positive going series Resistance is (R = 500 + 680 = 1180 ohms) and the Negative going series Resistance is (R = 500 + 200 (transistor) = 700 ohms). The smaller negative resistor should make the negative slope "more linear". Do you notice a difference in the linearity of the positive and negative slope?

Ed-Lab	HIGH PASS R - L NETWORK	EXP. NO. 18 Page No. 1

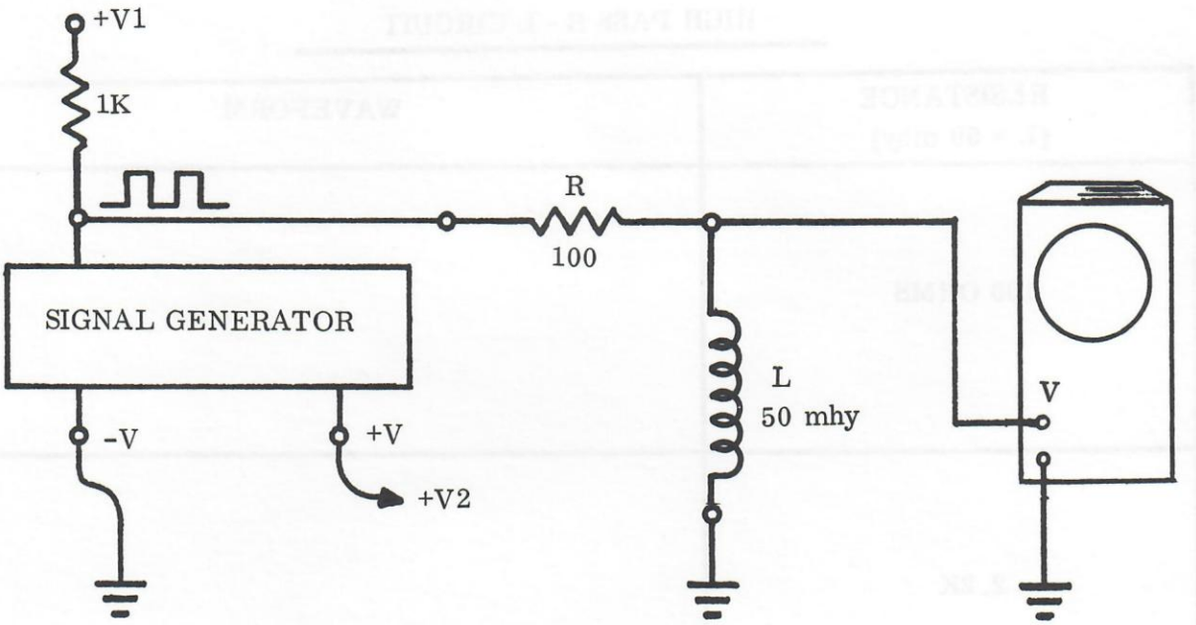


Figure 18 - 1 High Pass R - L Network

Objective:

You will observe the operation of a High Pass R - L network.

Description:

The High Pass R - L network has a pulse response similar to the high pass R - C network. The time constant is the same as the R - L low pass:

$$\tau = \frac{L}{R}$$

There are some very interesting results for high values of R where the "stray capacitances" result in oscillating conditions.

Procedure:

1. Wire the circuit in Figure 18 - 1.
2. Observe the results on the oscilloscope. Set the oscilloscope as in the previous experiment.
3. Substitute various resistors and observe the results and sketch the waveforms in the chart.

Ed-Lab	HIGH PASS R - L NETWORK	EXP. NO. 18 Page No. 2

HIGH PASS R - L CIRCUIT

RESISTANCE (L = 50 mhy)	WAVEFORM
100 OHMS	
2.2K	
10K	
100K	
1M	

Observe that you will obtain severe oscillations with the 100K resistance and higher resistors. This is due to the external STRAY CAPACITANCE across the coil resulting from the long wires and the input to the oscilloscope. This CAPACITANCE, C, creates a Parallel Resonance circuit, and the frequency of oscillation is:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

If the stray capacitance is 20 pfd, the resonant frequency will be:

$$f = \frac{1}{2\pi\sqrt{50\ 10^{-3}\ \text{x}\ 20\ 10^{-12}}}$$

$$= \frac{1}{2\pi\sqrt{10^{-12}}}$$

$$= \frac{1}{2\pi\ 10^{-6}}$$

$$f = 150,000 \text{ HERTZ}$$

4. Using the oscilloscope, measure the oscillation frequency.

FREQUENCY =	hertz

5. Calculate or estimate the Stray Capacitance, C.

C = pfd

Where:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$f^2 = \frac{1}{(2\pi)^2 LC}$$

$$C = \frac{1}{(2\pi)^2 \quad L \quad f^2}$$

$$C = \frac{1}{(6.28)^2 \quad (50\ 10^{-3}) \quad f^2}$$

$$C = \frac{1}{2\ f^2}$$

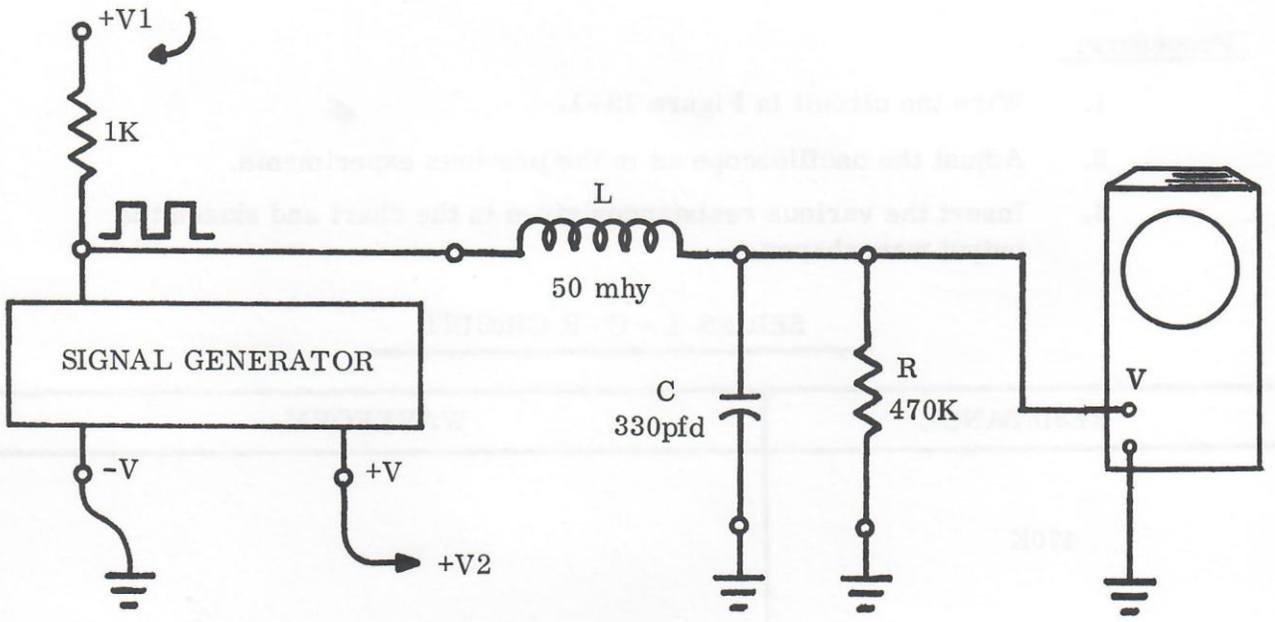


Figure 19-1 L-C-R Circuit

Objective:

You will observe the output when a Pulse is transmitted to an L-C-R Circuit. You will test the requirement for LOADING.

Description:

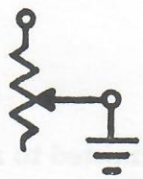
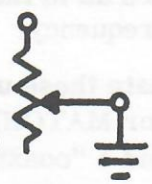
When high frequency pulses are transmitted from one circuit to another circuit, the wires act as "distributed" Inductors and Capacitors simplified above as a single inductor and capacitor. The same result occurs as in the previous experiment and oscillations occur at the series resonant frequency.

A resistor at the load, R, must be used to eliminate these unwanted oscillations. Such a resistor is called a LOAD Resistor (or MATCHING resistor). When using high frequency test instruments, and a "coaxial cable", a matching resistor of 50 ohms is frequently used.

Procedure:

1. Wire the circuit in Figure 19-1.
2. Adjust the oscilloscope as in the previous experiments.
3. Insert the various resistances given in the chart and sketch the output waveshapes.

SERIES L - C - R CIRCUIT

RESISTANCE	WAVEFORM
470K	
100K	
100K POT (Vary) 	
3.3K	
10K POT (Vary) 	
1K	

4. Which size matching resistor would you select?

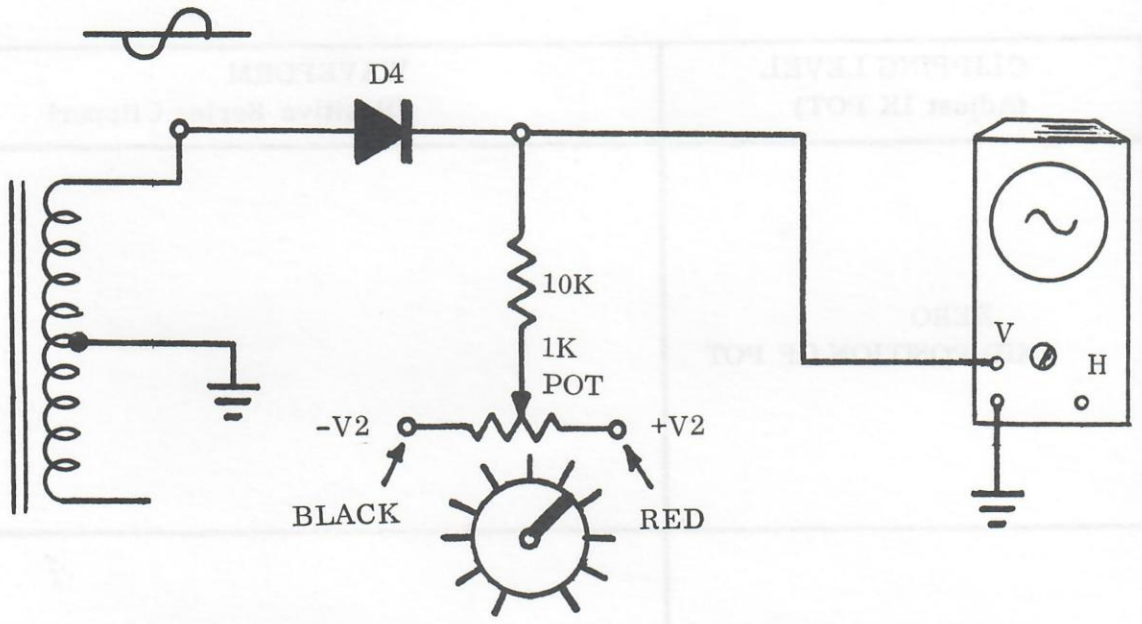


Figure 20 - 1 Series Positive Diode Clipper

Objective:

You will use a SERIES DIODE in a Clipping circuit and vary the bias to adjust the clipping level.

Description:

The series diode circuit above is the same as the HALF-WAVE RECTIFIER. The "return-voltage" is not connected to ground but rather connected a variable voltage source; the 1K POT between +V2 and -V2. Adjusting this voltage will adjust the CLIPPING LEVEL. The applied signal is the 60 hertz voltage from the transformer. This circuit will operate with any input signals or pulses.

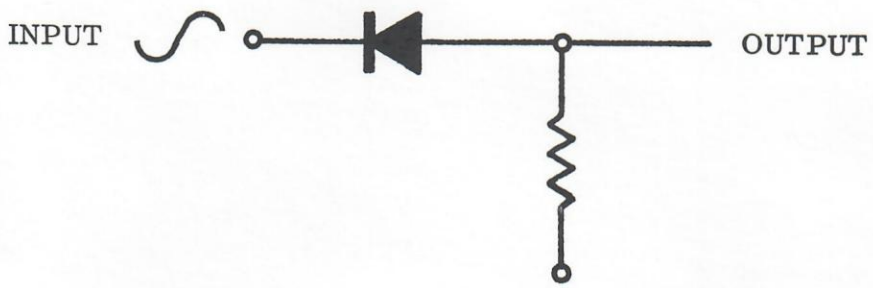
Procedure:

1. Wire the circuit in Figure 20 - 1.
2. Adjust the oscilloscope with the zero (ground) level at the center and approximately 2 or 3 cycles across the oscilloscope face.
3. Set the 1K POT at the center.

4. Sketch the wave shapes at various clipping levels.

CLIPPING LEVEL (Adjust 1K POT)	WAVEFORM (Positive Series Clipper)
ZERO MID POSITION OF POT	
LOW (Negative Voltage) (POT NEAR -V2) Counter Clockwise	
HIGH (Positve Voltage) (Rotate POT Clockwise)	

5. Reverse the direction of the DIODE.



The circuit is now a NEGATIVE SERIES DIODE CLIPPER.

6. Sketch some waveforms below:

CLIPPING LEVEL (Adjust 1K POT)	WAVEFORM (Negative Series Clipper)
ZERO	
LOW (Negative Voltage)	
HIGH (Positive Voltage)	

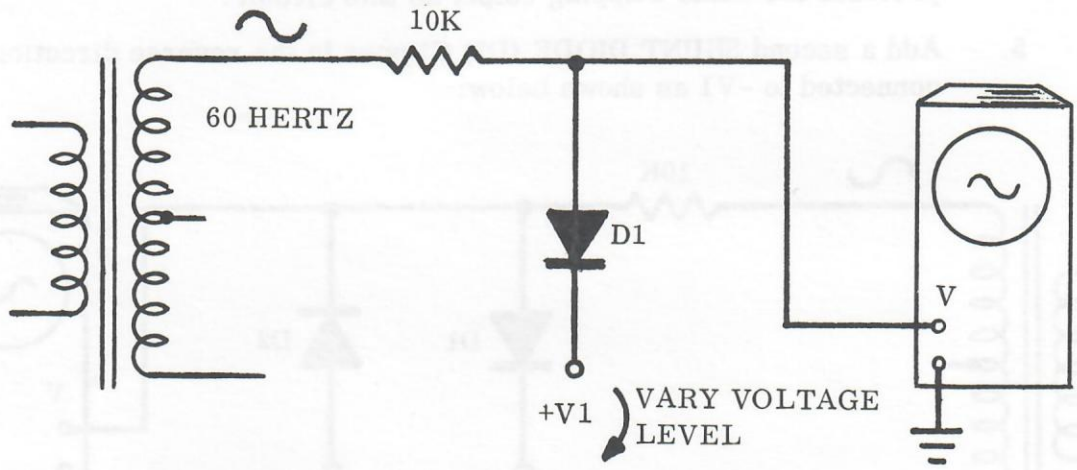


Figure 21 - 1 Shunt Diode Clipper

Objective:

You will use a Shunt or Parallel Diode as a Clipper and then use two shunt clippers for positive and negative clipping.

Procedure:

1. Wire the above circuit.
2. Vary the clipping voltage (+V1 Power Supply) and observe the results.
3. Sketch some waveforms below:

+V1 = 0	+V1 = mid (+5v)	+V1 = high (+9v)

4. Which Series Diode Clipping circuit from the previous experiment provides the same Clipping output as this circuit?

5. Add a second SHUNT DIODE (D2) Clipper in the reverse direction connected to -V1 as shown below:

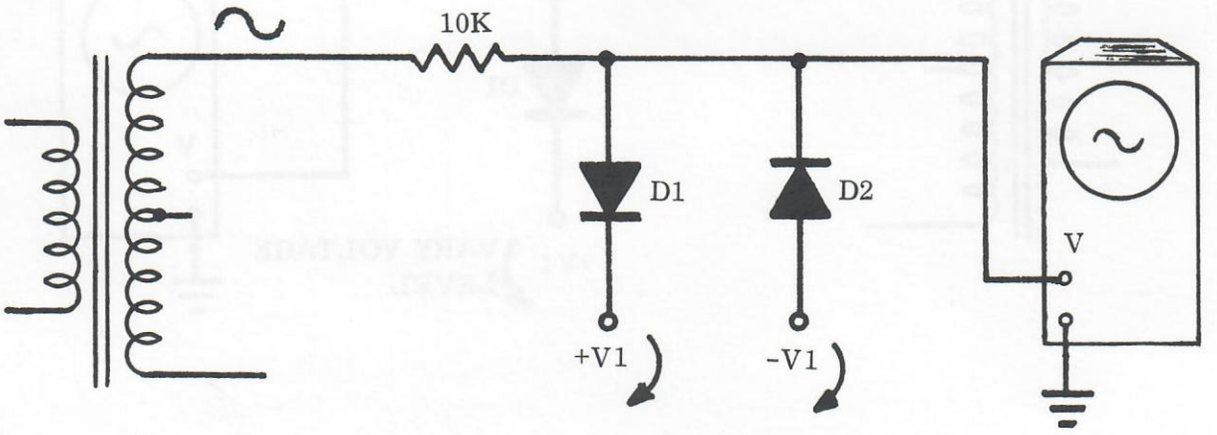


Figure 21 - 2 Two Level Clipping

Vary +V1 and -V1 and observe the results.

6. Adjust +V1 and -V1 to mid point and plot the douple clipped signal below:

The Shunt Clipping circuit provides a capability for clipping both positive and negative ends of signals.

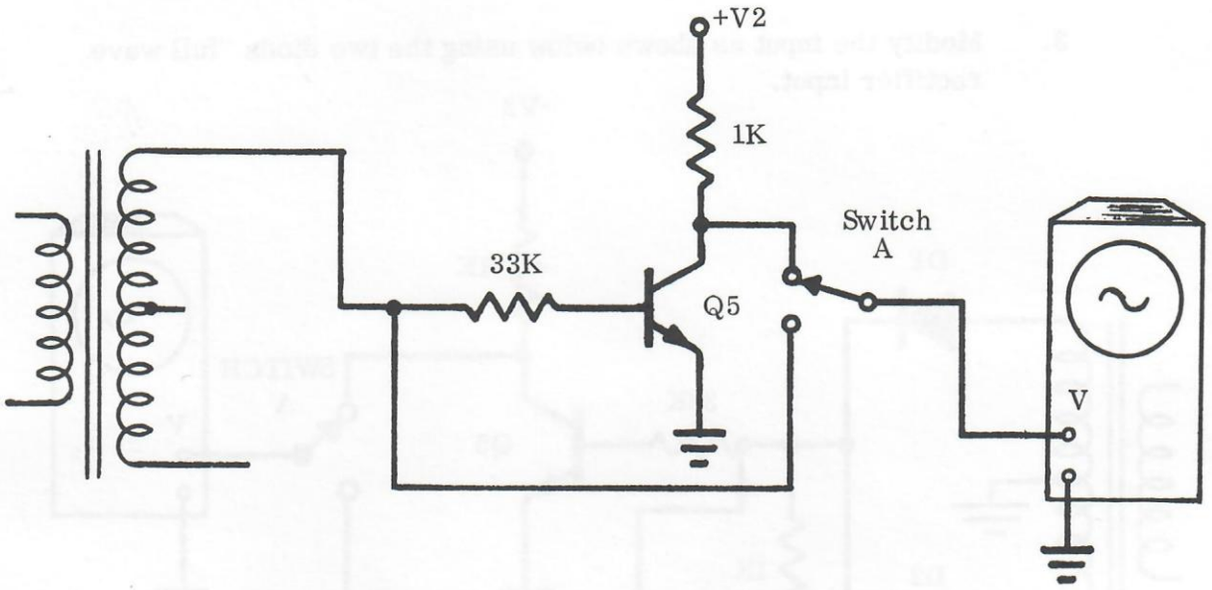


Figure 22 - 1 Transistor Clipper

Objective:

You will use a transistor amplifier to CLIP and SQUARE the input signal. This transistor circuit is an ACTIVE waveshaping circuit.

Procedure:

1. Wire the circuit in Figure 22 - 1. The high input signal drives the transistor full ON and full OFF. The output is then a CLIPPED and AMPLIFIED signal or a SQUARED-OFF signal.

2. Observe the output on the oscilloscope and plot the input and output waveforms.

INPUT

SWITCH A DOWN

CLIPPED OUTPUT

SWITCH A UP

3. Modify the input as shown below using the two diode "full wave rectifier input.

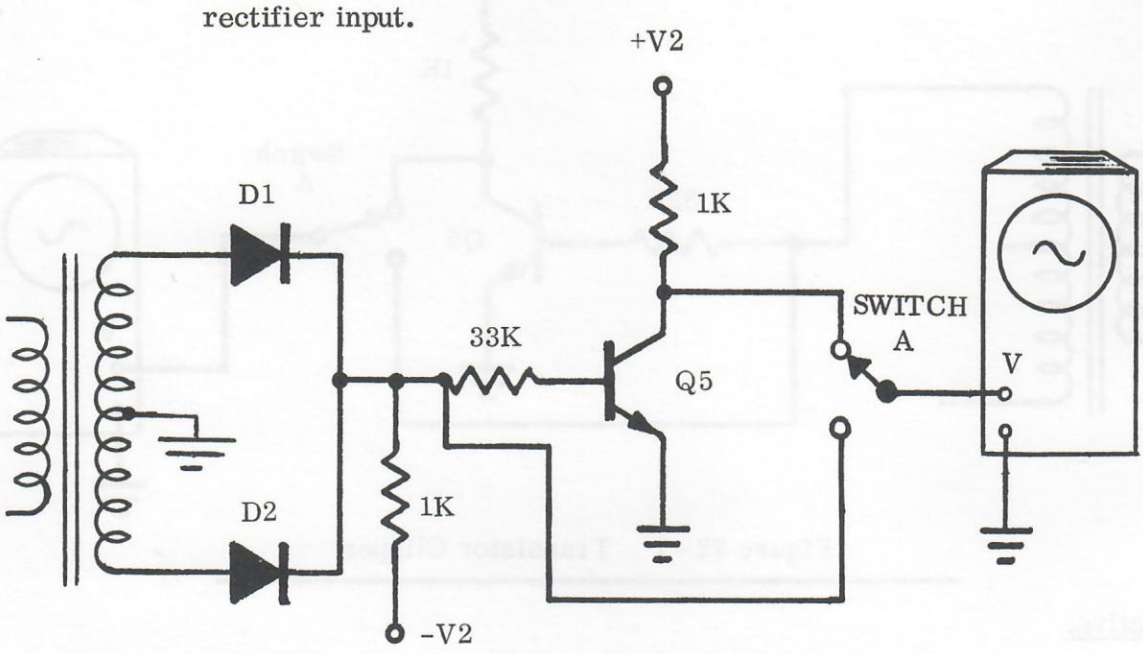


Figure 22 - 2 Full Wave Rectifier/Clipper

4. Plot the input and output as observed for Figure 22 - 2.

INPUT
Switch A
DOWN

OUTPUT
Switch A
UP

The above signal provides accurate timing pulses obtained from the 60 hertz power line. What is the frequency of the pulses?

Ed-Lab | DIODE PULSE CLAMPING | EXP. NO. 23 Page No. 1

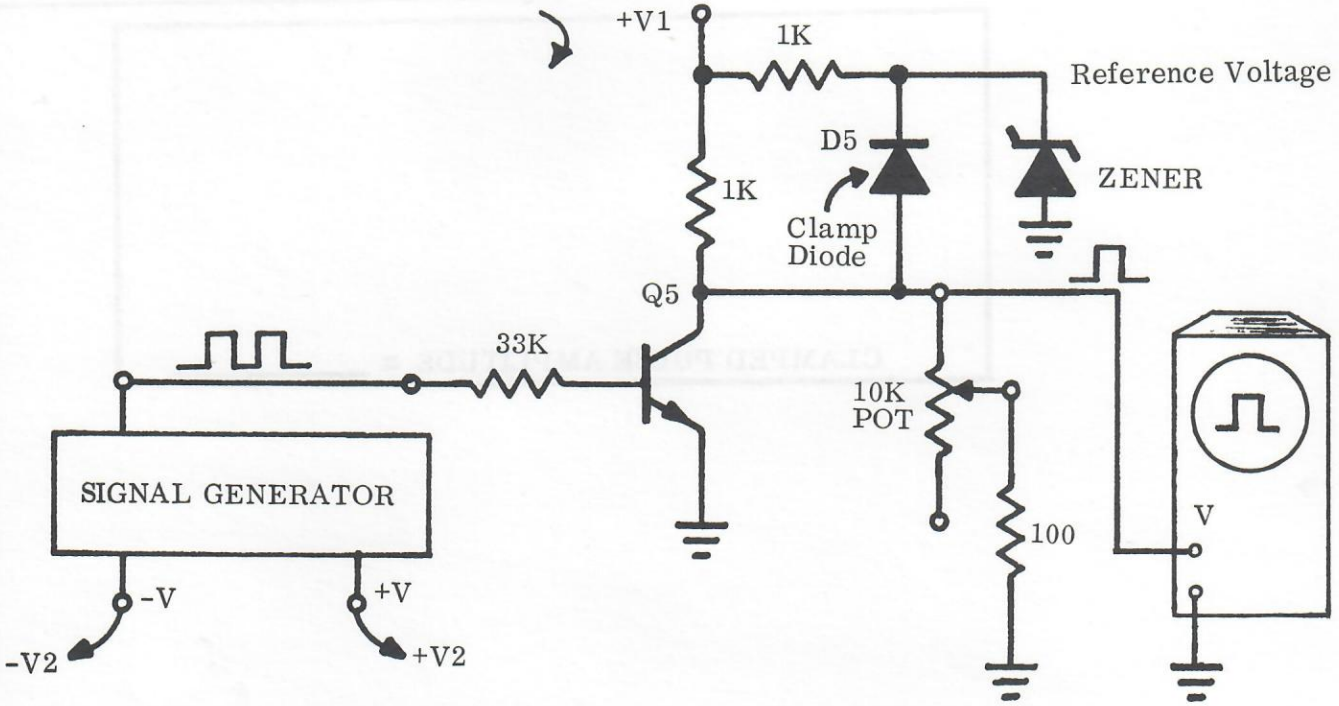


Figure 23 - 1 Diode Pulse Clamping

Objective:

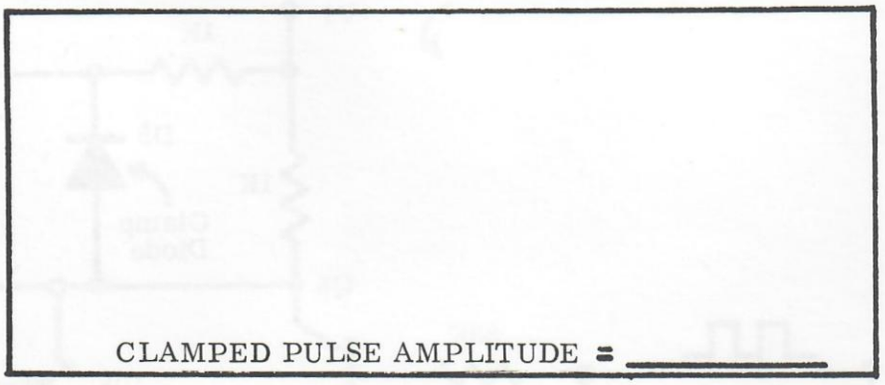
You will use a diode to CLAMP (or CLIP or LIMIT) the top of a pulse signal derived from the output of a common emitter amplifier in a circuit designed to maintain a constant amplitude independent of load.

Description:

In a previous experiment (Pulse Circuit Loading - Experiment No. 14), it was demonstrated how Resistor Loads, from the collector output to ground, changed the output pulse level due to the simple resistor voltage divider circuit. In many cases, it is necessary to maintain a constant pulse amplitude. This diode clipping circuit is called a CLAMP. The pulse clamp-voltage is set by the ZENER diode circuit. The pulse will maintain the steady amplitude independent of load except for very low load resistors where the voltage-divider output voltage would be below the zener "clamp voltage".

Procedure:

1. Wire the circuit in Figure 23 - 1. The load consists of the 100 ohm resistor in series with the 10K POT.
2. Vary the 10K POT and observe that the output peak voltage does not vary. Sketch the Pulse showing pulse amplitude:



CLAMPED PULSE AMPLITUDE = _____

3. Remove the clamping diode D5. Vary the 10K POT Load and observe the variation in pulse amplitude without the clamping diode. What is the maximum amplitude or un-clamped pulse amplitude at the full 10K load?

UNCLAMPED PULSE AMPLITUDE =

Ed-Lab	D. C. RESTORER	EXP. NO. 24 Page No. 1

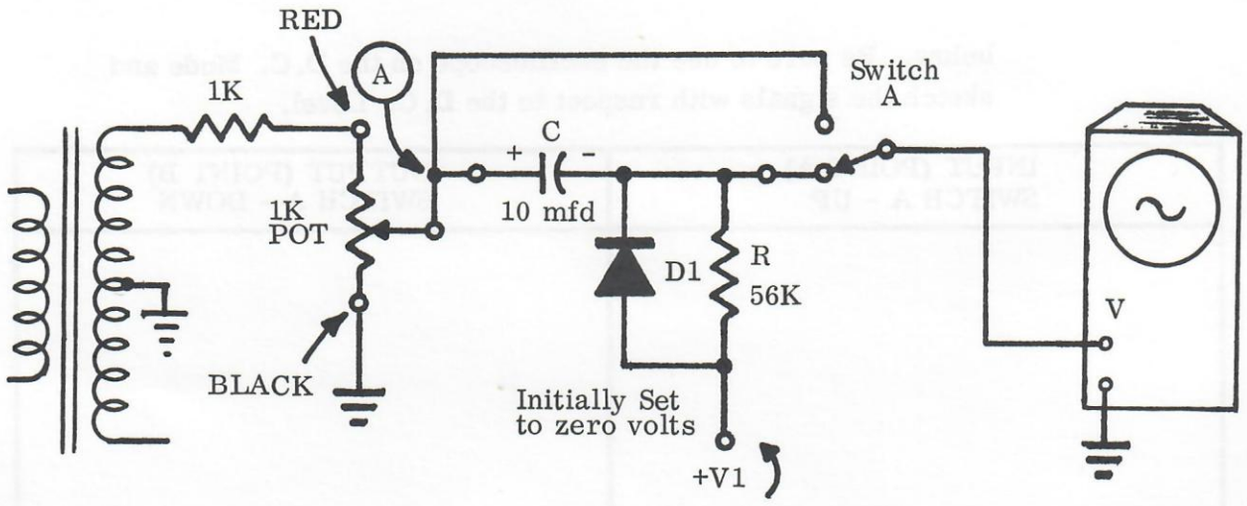


Figure 24 - 1 D.C. Restorer

Objective:

You will use a series Capacitor-Diode Circuit to control the D.C. Level of a signal.

Description:

When the input signal at point A is negative with respect to ground, diode D1 conducts and the Capacitor changes quickly to the negative voltage. When the voltage level at point A rises, the Capacitor cannot discharge through the diode which is in the reverse direction and the voltage across the capacitor has the effect of a SERIES BATTERY. The lowest output voltage then "rests" above ground at all times or is RESTORED to a ground D.C. level.

Procedure:

1. Wire the circuit in Fugure 24 - 1.

   Be sure that Voltage +V1 is set at zero (Maximum counter clockwise).
   Set the 1K POT to maximum signal.

2. Observe the input and output on the oscilloscope. Sketch the waveforms

below. Be sure to use the oscilloscope on the D.C. Mode and sketch the signals with respect to the D.C. Level.

INPUT (POINT A) SWITCH A - UP	OUTPUT (POINT B) SWITCH A - DOWN

3. Vary +V1 to positive voltages. Observe that the output (point B, Switch A DOWN) level varies.

4. Set +V1 back to ground (maximum counter clockwise). Vary the input amplitude by adjusting the 1K POT. Observe that the signal bottom re-adjusts to zero volts or RESTORES A ZERO D.C. VOLTAGE to the lowest level of the waveform.

Ed-Lab | A.C. SOLID-STATE VOLTMETER | EXP. NO. 25 Page No. 1

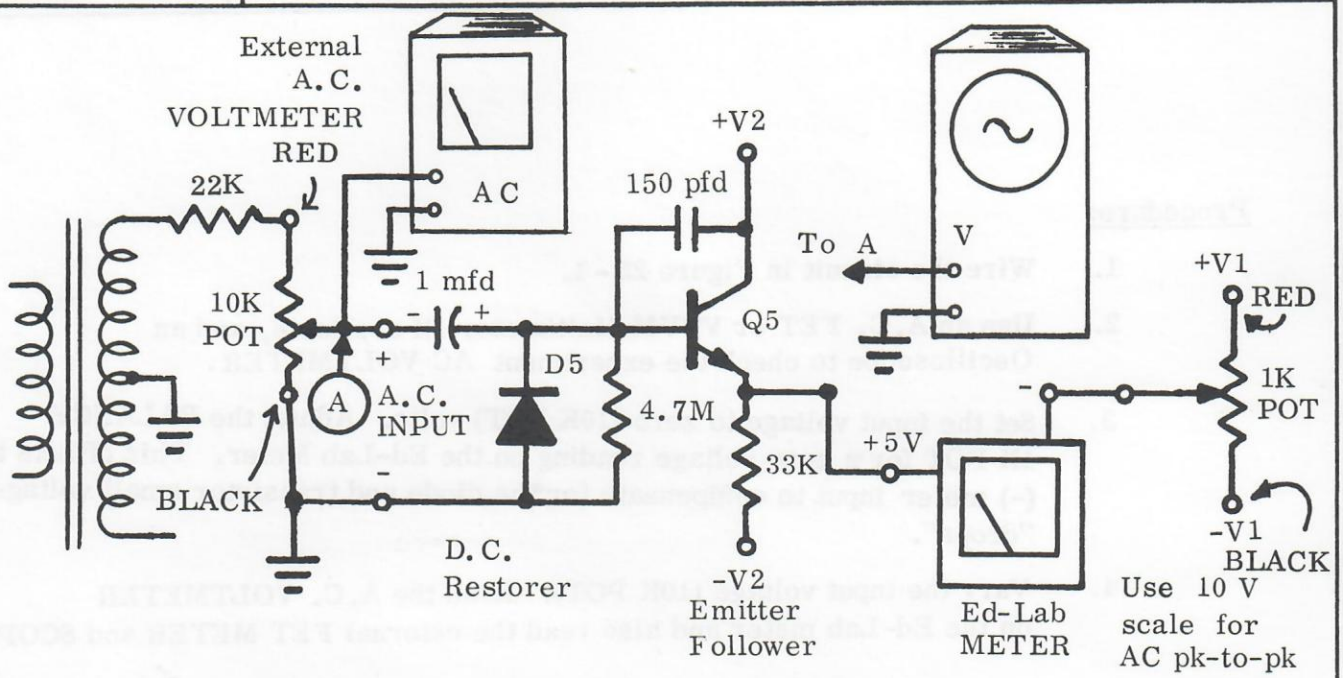


Figure 25 - 1 A.C. VOLTMETER

Objective:

You will use a D.C. Restorer with the D.C. Meter to build an A.C. SOLID-STATE VOLTMETER.

Description:

The 10K POT provides for a variation in input AC voltage amplitude at point (A). The D.C. Restorer provides an all positive voltage for the D.C. Meter. The D.C. Meter will read the AVERAGE D.C. VOLTAGE. The transistor emitter-follower is used to provide a High-Input Resistance (Impedance) so that the meter will not "load" the circuit where the voltage is being measured.

The input AC sinewave is restored to where the negative peak of the sinewave is at the zero voltage level. The average voltage is slightly lower than the middle of the sinewave. The DC reading on the DC Meter corresponds to this average voltage. The Peak-to-Peak voltage is approximately twice the average voltage. Therefore, when using the meter with the +5 volt D.C. Input, we read the +10 Volt scale for AC Peak-to-Peak voltages. Similarly, when reading the Ed-Lab Meter with the +0.5 V DC scale, we can read this Ed-Lab Meter as a 1 Volt AC Peak-to-Peak Scale Meter. There may be some "clipping" distortion on the bottom of the sine wave resulting from the restorer diode conduction.

Ed-Lab	A.C. SOLID-STATE VOLTMETER	EXP. NO. 25 Page No. 2

Procedure:

1. Wire the circuit in Figure 25 - 1.
2. Use an A.C. FET or VTVM Multimeter, if available, and an Oscilloscope to check the experiment AC VOLTMETER.
3. Set the input voltage to zero (10K POT) volts. Adjust the BALANCE 1K POT for a zero voltage reading on the Ed-Lab Meter. This offsets the (-) meter input to compensate for the diode and transistor small voltage "drops".
4. Vary the input voltage (10K POT). Read the A.C. VOLTMETER on the Ed-Lab meter and also read the external FET METER and SCOPE.

Enter the results below:

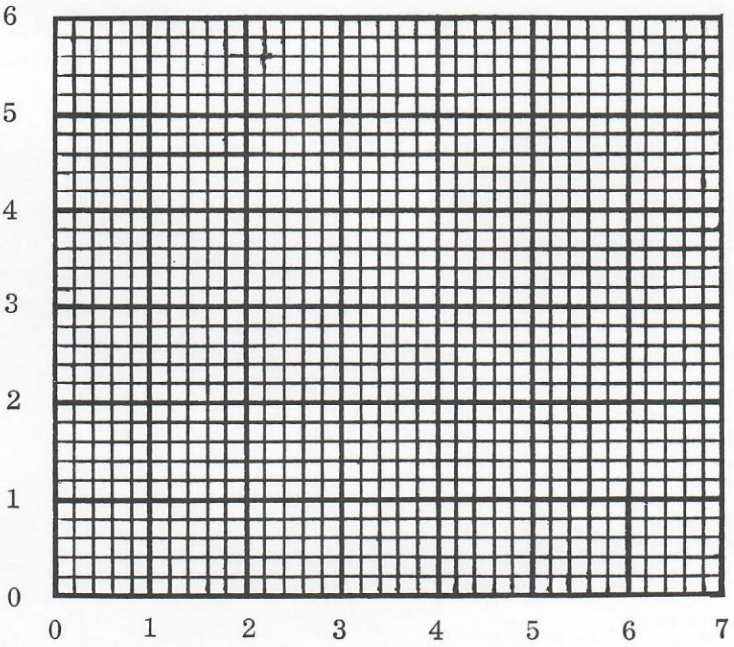
(peak-to-peak)

POT POSITION	A.C. VOLTMETER ED-LAB METER	OSCILLOSCOPE (Peak-to-Peak)	AC METER EXTERNAL
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

5. Plot the results below:

1. EXTERNAL A.C. METER (peak-to-peak)

2. SCOPE (Peak-to-Peak)



Ed-Lab A.C. Voltmeter

6. Comment on the comparisons.

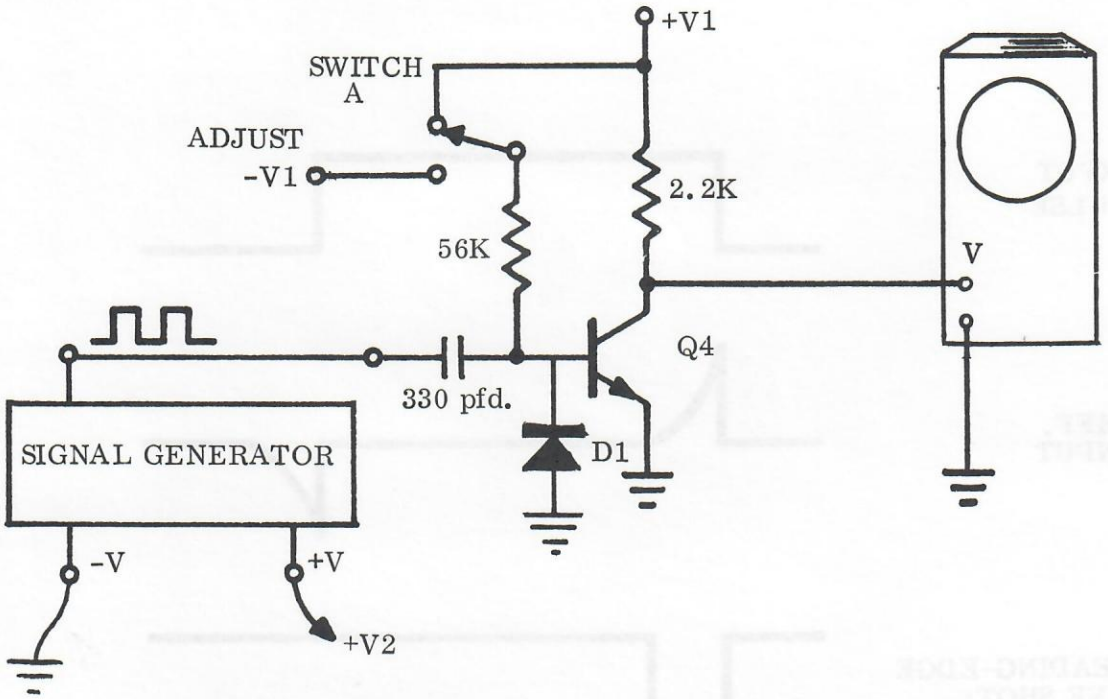


Figure 26 - 1 Pulse Compressor

Objective:

You will use an RC Differentiator Circuit (PASSIVE WAVESHAPING circuit) together with a Transistor to yield an ACTIVE WAVESHAPING circuit called a PULSE COMPRESSOR. This circuit can be "biased" to be a LEADING-EDGE ONE-SHOT or a TRAILING-EDGE ONE-SHOT. AMonostable Multivibrator has two transistors and is also called a ONE-SHOT. The above circuit uses one transistor and is sometimes called a HALF-SHOT. The Trailing-Edge-One-Shot is sometimes called a DELAY.

Description:

The RC circuit (330 pfd and 56K) is a Differentiator with short positive and negative output pulses. The transistor circuit has a 56K bias resistor which is connected to either plus-volts (Switch A UP) or minus-volts (Switch A DOWN).

The plus-bias results in an ON transistor with zero volts output. The negative differentiated pulses turn the transistor OFF yielding a short positive output pulse.

The negative-bias (Switch A DOWN) results in an OFF transistor with a plus volts output. The positive differentiated pulses turn the transistor ON resulting in a short negative pulse. When a single wide input pulse is applied as an input, the outputs appear as shown on the following page:

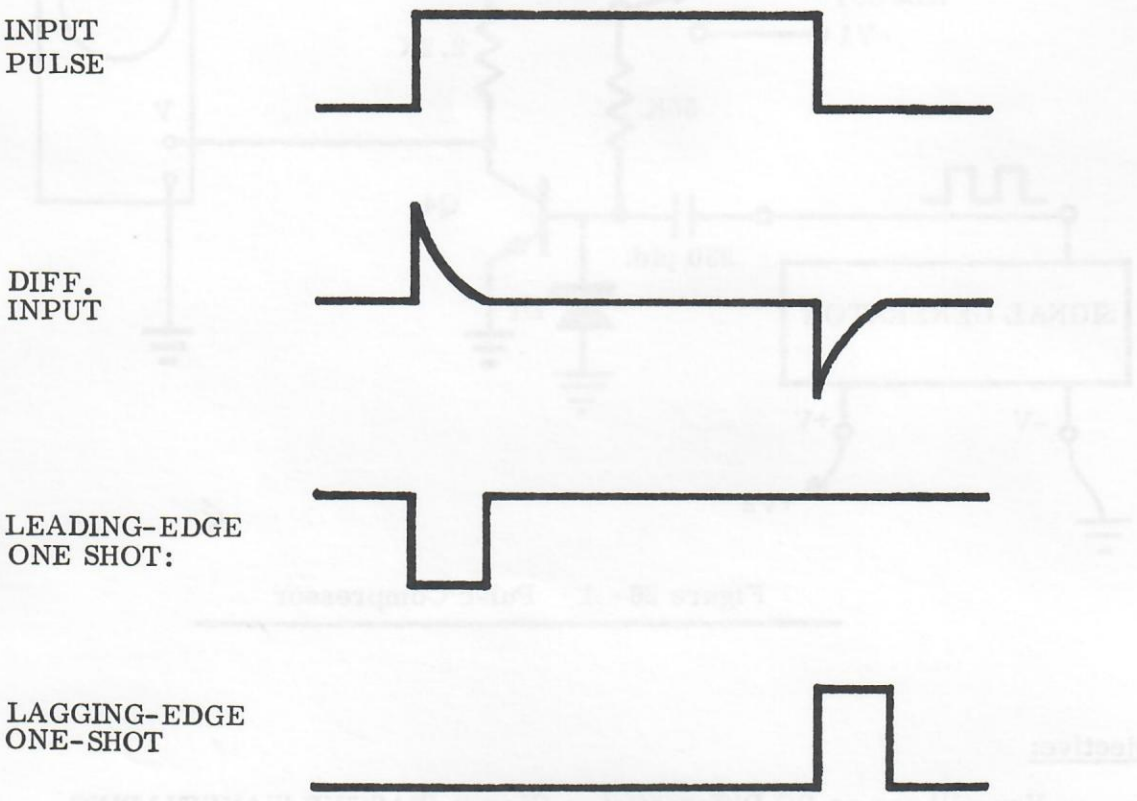


Figure 29 - 2 Pulse Compressor (One-Shot) Waveforms

The Lagging-Edge One-Shot results in an output at the end of the pulse and is also called a DELAY circuit.

Procedure:

1. Wire the circuit in Figure 26 - 1.
2. Observe the outputs and enter the results below:
   Place Switch A DOWN, adjust -V1 until pulse amplitude just begins to decrease.
3. Observe output and enter results on the next page.

PULSE COMPRESSOR OUTPUTS

SWITCH A - UP

SWITCH A - DOWN

4. Which outputs above correspond to the Leading-Edge and Lagging-Edge One-Shots?

Ed-Lab | PULSE STRETCHER | EXP. NO. 27 Page No. 1

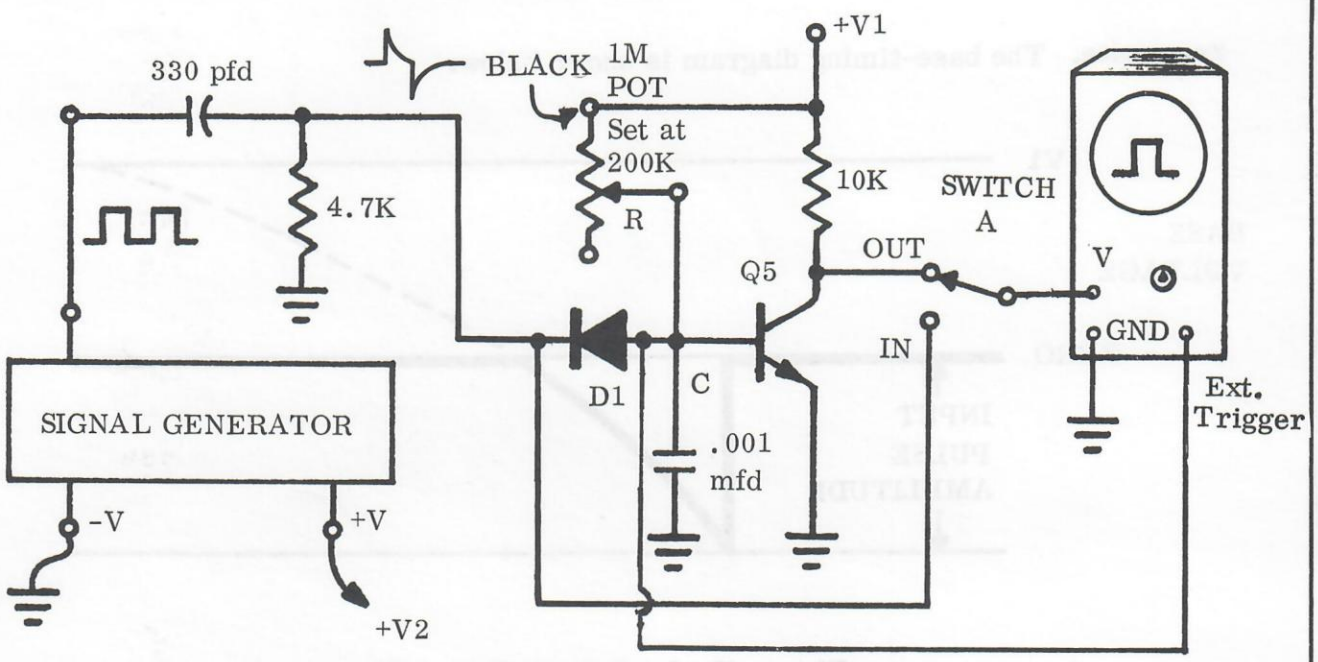


Figure 27 - 1 Pulse Stretcher

Objective:

You will use DIODE R - C TIMING CIRCUIT to result in a PULSE STRETCHER Active Waveshaping Circuit.

Description:

The standard R - C Differentiator (330 pfd, 4.7K) results in positive and negative "spikes". We are only considering the negative pulses which are used as the input signals. This R - C Circuit provides the short input negative pulses and is not part of the Pulse Stretcher Circuit.

The Transistor is biased ON with the Base Resistor (1M POT) set at approximately 200K ohms. The transistor output is thus zero volts.

The Diode permits the negative pulse to charge the Capacitor (.001 mfd) to a negative voltage which turns the transistor OFF resulting in a positive output voltage.

The negative voltage "charges" to a positive voltage (+V1) with a time constant (RC). When this voltage at the base of the transistor reaches zero volts or slightly positive, the transistor turns ON again, and the output becomes

zero volts. The base-timing diagram is shown below:

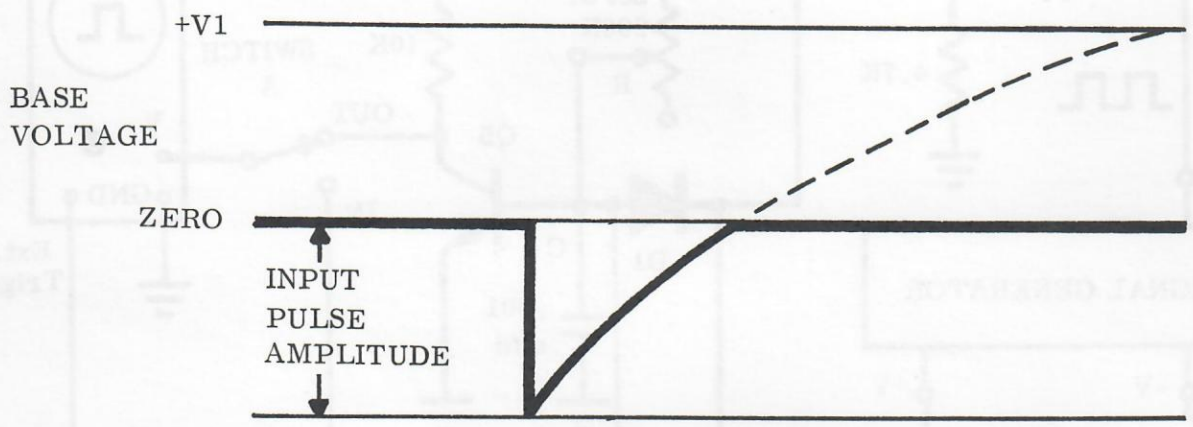


Figure 27 - 2 Base Voltage - Timing

Procedure:

1. Wire the circuit in Figure 27 - 1. Set Scope to External Trigger.
2. Observe the output on the oscilloscope with Switch A UP.
3. Vary the 1M POT and observe the output "stretched" pulse. Sketch the waveform below for R = 200K. What is the pulse width?

OUTPUT / SWITCH A UP	
INPUT / SWITCH A DOWN	

4. Vary the 1M POT and comment on the pulse width.

1M POT SETTING	PULSE WIDTH
100K	
200K	
300K	
400K	
700K	
900K	

5. What happens as R increases (the POT Resistance)?

Ed-Lab		UNIT NO. 10 EXP. NO. 32 Page No. 2.2

Ed-Lab	CAPACITOR - DIODE GATE	EXP. NO. 28 Page No. 1

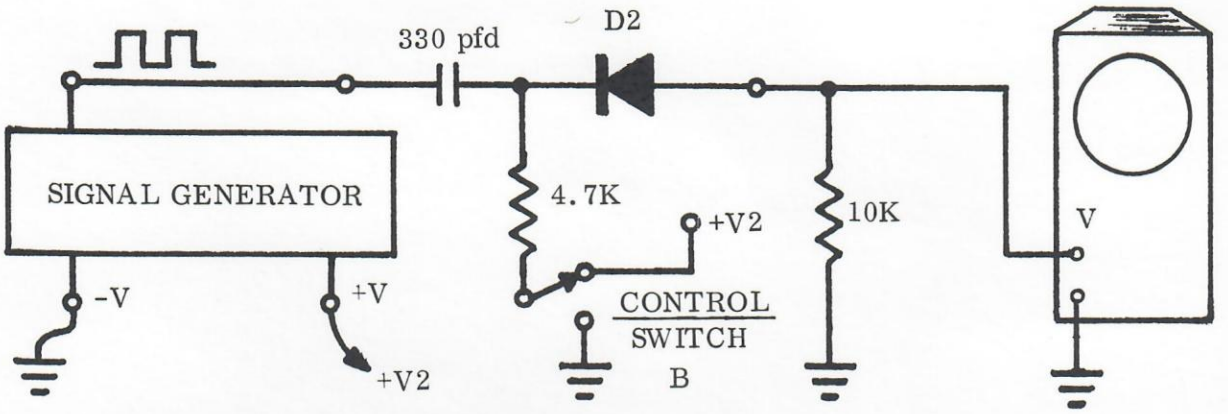


Figure 28 - 1 C - D GATE

Objective:

You will use a Capacitor - Diode - Resistor Circuit to act as a GATE to enable the transfer of negative pulses to the output. This circuit is used to control input Triggers to Multivibrators.

Description:

When Switch B is UP, a positive voltage (+V2) "reverse biases" the diode, D2, and pulses are not "gated" to the output.

When Switch B is DOWN, the resistor is "grounded". The C and R components are a "differentiator and generate short positive and negative pulses. The negative pulses then appear at the output.

Procedure:

1. Wire the circuit in Figure 28 - 1.
2. Observe the outputs on the oscilloscope and sketch the results below. Be sure to sketch the proper voltage of Bias levels.

OUTPUT (SWITCH B UP)	OUTPUT (SWITCH B DOWN)

Ed-Lab	TRIGGERED FLIP-FLOP	EXP. NO. 29 Page No. 1

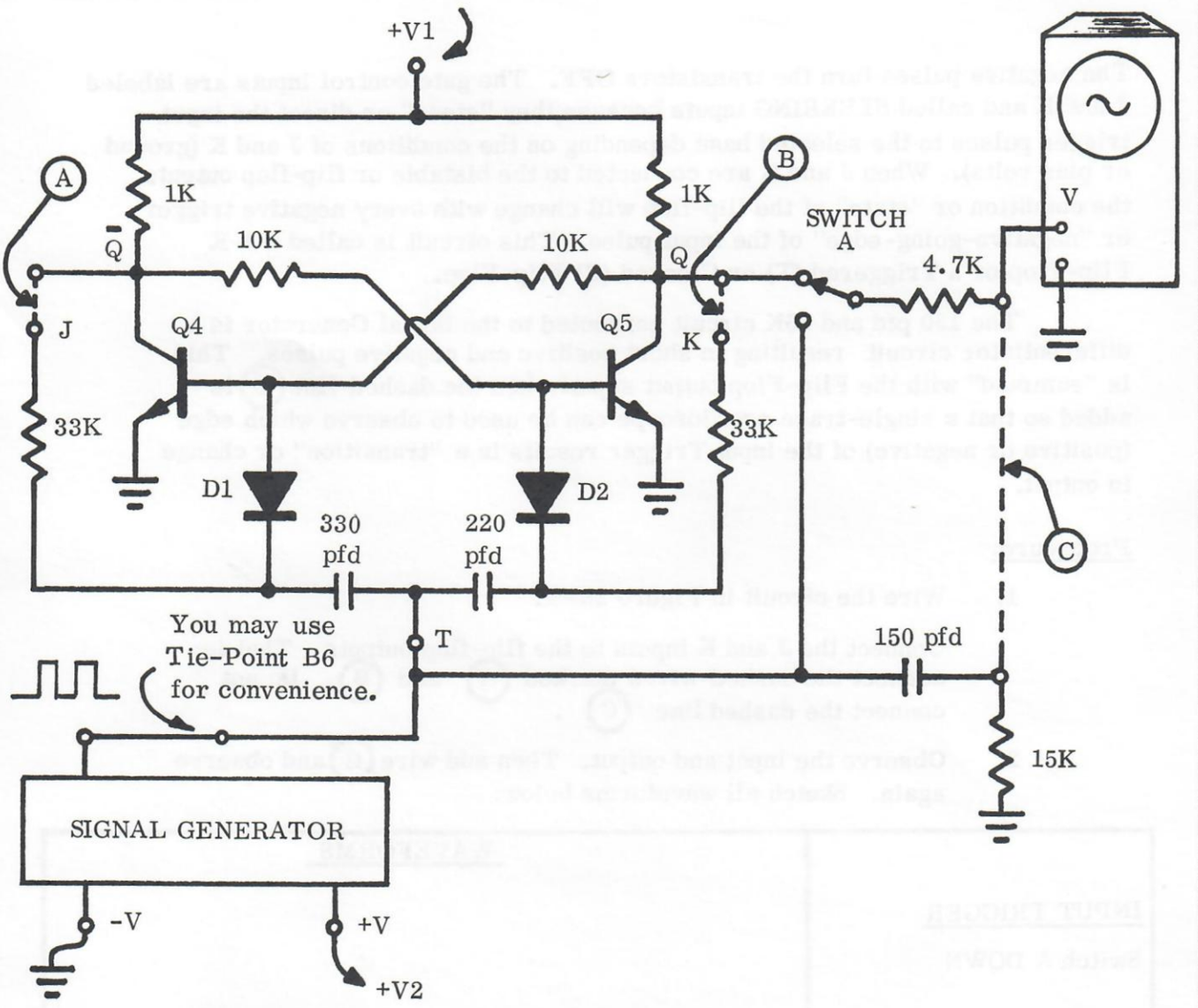


Figure 29 - 1 Triggered Flip-Flop

Objective:

You will connect two C-D Gates to a Bistable Multivibrator to result in a J-K Steered Flip-Flop and a Triggered Flip-Flop.

Description:

Two C-D Gates are connected with a common-input called the TRIGGER (T) and with the outputs connected to the transistor bases of a bistable multivibrator.

The negative pulses turn the transistors OFF. The gate control inputs are labeled J and K and called STEERING inputs because they "steer" or direct the input trigger pulses to the selected base depending on the conditions of J and K (ground or plus volts). When J and K are connected to the bistable or flip-flop outputs, the condition or "state" of the flip-flop will change with every negative trigger or "negative-going-edge" of the input pulse. This circuit is called a J-K Flip-Flop or a Triggered (T) or Clocked (C) Flip-Flop.

The 150 pfd and 15K circuit connected to the Signal Generator is a differentiator circuit resulting in short positive and negative pulses. This is "summed" with the Flip-Flop output signal when the dashed-line (C) is added so that a single-trace oscilloscope can be used to observe which edge (positive or negative) of the input Trigger results in a "transition" or change in output.

Procedure:

1. Wire the circuit in Figure 29 - 1.

   Connect the J and K inputs to the flip-flop outputs. That is; connect the dashed-wires marked (A) and (B). Do not connect the dashed line (C).

2. Observe the input and output. Then add wire (C) and observe again. Sketch all waveforms below:

	WAVEFORMS
INPUT TRIGGER Switch A DOWN	
FLIP-FLOP OUTPUT Switch A UP (Wire (C) not connected)	
FLIP-FLOP OUTPUT Switch A UP (Wire (C) connected)	

3. From the observations on the oscilloscope, which input edge triggers the flip-flop?

Ed-Lab | STAIRCASE GENERATOR | EXP. NO. 30 Page No. 1

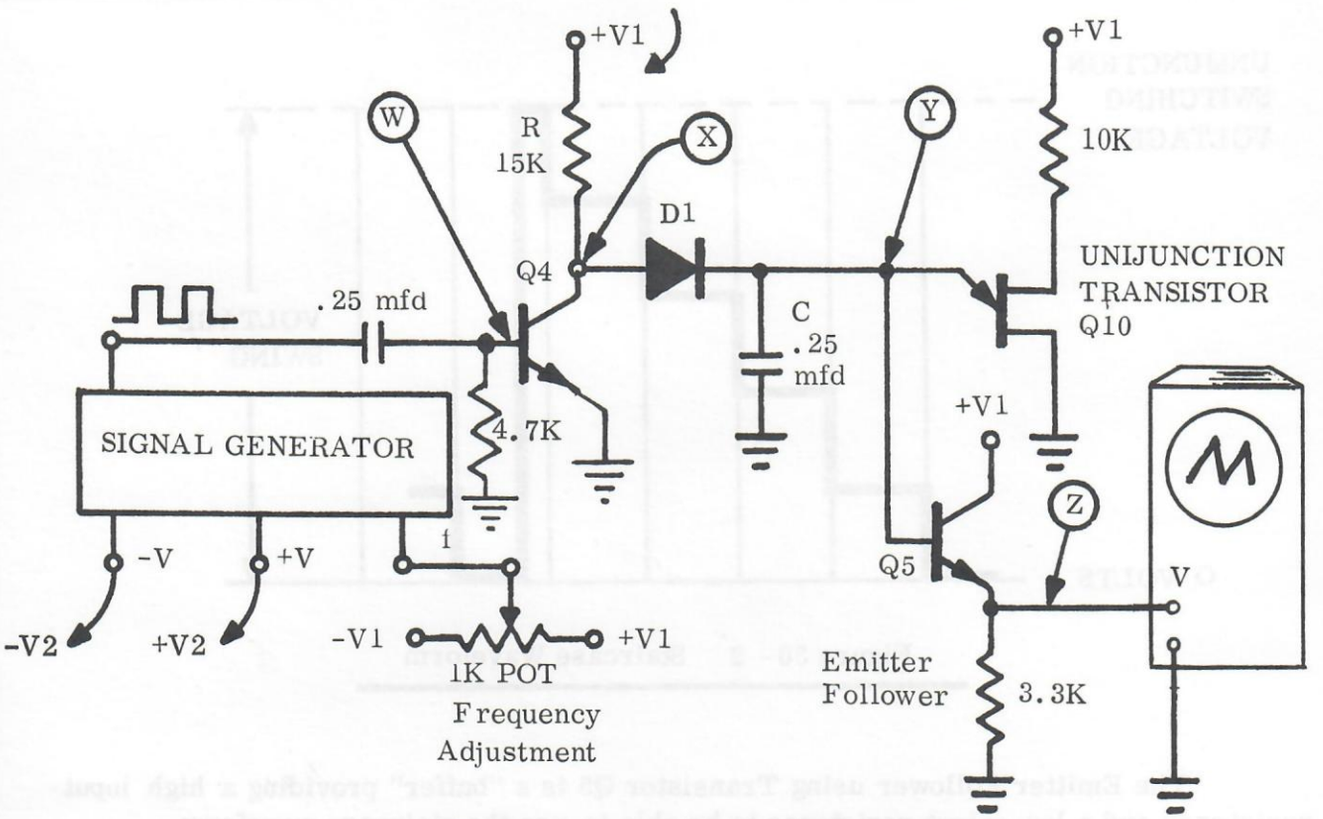


Figure 30-1 Staircase Generator

Objective:

You will use a Resistor-Diode-Capacitor Circuit as a STAIRCASE waveform generator which is another example of an Active Waveshaping Circuit.

Description:

The Signal Generator provides a square wave which is differentiated by the input .25 mfd cap, and the 4.7K resistor(Point W) , which together with Transistor Q4 form a One-Shot Pulser generating a short positive pulse at the output-collector of Q4 (Point X). The positive pulse charges the Capacitor, C, (.25 mfd) through the 15K Resistor and the Diode, D1. This is similar to the operation of the Pulse Stretcher. When the pulse level returns to zero volts, the diode is "backbiased" and the capacitor has no "path" to discharge the voltage and thus the voltage on the capacitor is retained. The next positive pulse charges the capacitor further with the same R-C Time Constant.

The Unijunction Transistor (Q10) is an "open circuit" until a certain fixed level is reached, at which time the input is switched to ground to discharge the capacitor. The resultant staircase waveform is shown on the following page. The Unijunction Transistor is studied in detail under another experiment.

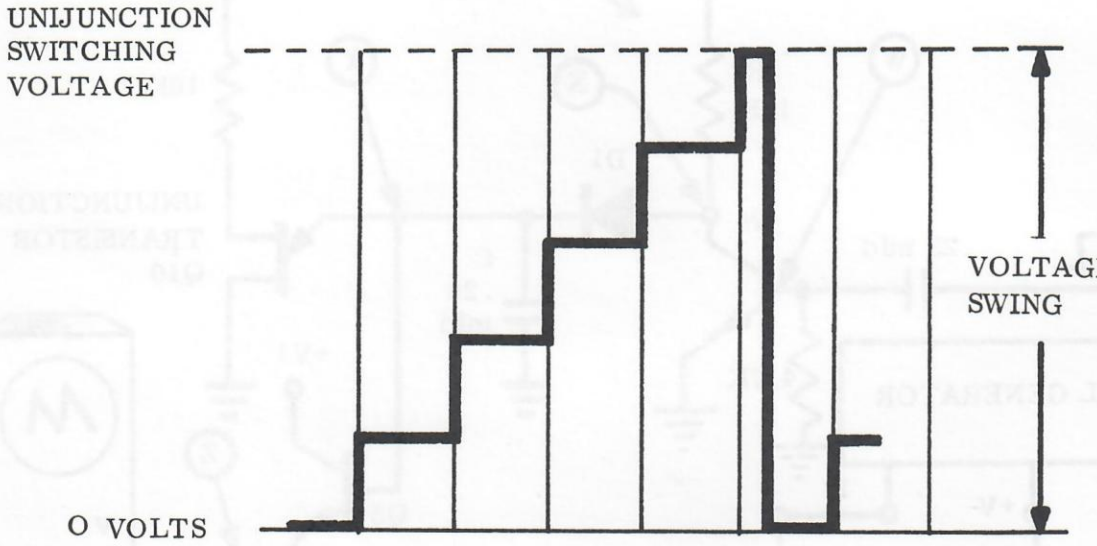


Figure 30 - 2 Staircase Waveform

The Emitter Follower using Transistor Q5 is a "buffer" providing a high input resistance and a low output resistance to be able to use the staircase waveform to "drive" another circuit without providing a "discharge-path" for the capacitor voltage or capacitor "charge".

The Signal Generator pulse frequency is varied by the 1K POT.

Procedure:

1. Wire the circuit in Figure 30 - 1.
2. Use the Oscilloscope to observe the waveforms at Point Y , and adjust the pulse frequency (1K POT) for a small number of steps (4 or 5).

3. Sketch the waveforms at points (W), (X), (Y), (Z) below:

(W)

(X)

(Y)

(Z)

4. Indicate the waveform Period, Step Size (Voltage), Overall Voltage Sweep, and other factors below and experiment with the circuit to determine the answers to questions 5, 6, 7, 8, 9, and 10.

NUMBER OF STEPS	(Use Oscilloscope)
PERIOD	
STEP-SIZE (Volts)	
VOLTAGE SWING	

5. Does the PERIOD change when the frequency is varied?
6. What circuit components determine the Period?
7. What determines the number of steps?
8. What determines the step voltage-amplitude?
9. What determines the voltage-swing?
10. What are the maximum and minimum number of steps that can be obtained?

Refer to Figure 30-3 on the following page.

The A.C. 60 Hertz Transformer is used as the input signal and frequency. Diodes D1 and D2 provide a rectified signal, point (A) which generates a short positive pulse on the silicon transistor (Q7) collector output. The charging R-C circuit consists of the 10K POT and the 5 mfd Capacitor in the 60 Hertz Staircase Generator circuit.

11. Wire the circuit in Figure 30-3. Monitor the output on the oscilloscope. Adjust the 10K POT to control the charging time-constant. Tabulate the Number of Steps, Period, Step Size, Voltage Sweep and Sweep Frequency.

Ed-Lab | STAIRCASE GENERATOR | EXP. NO. 30 Page No. 5

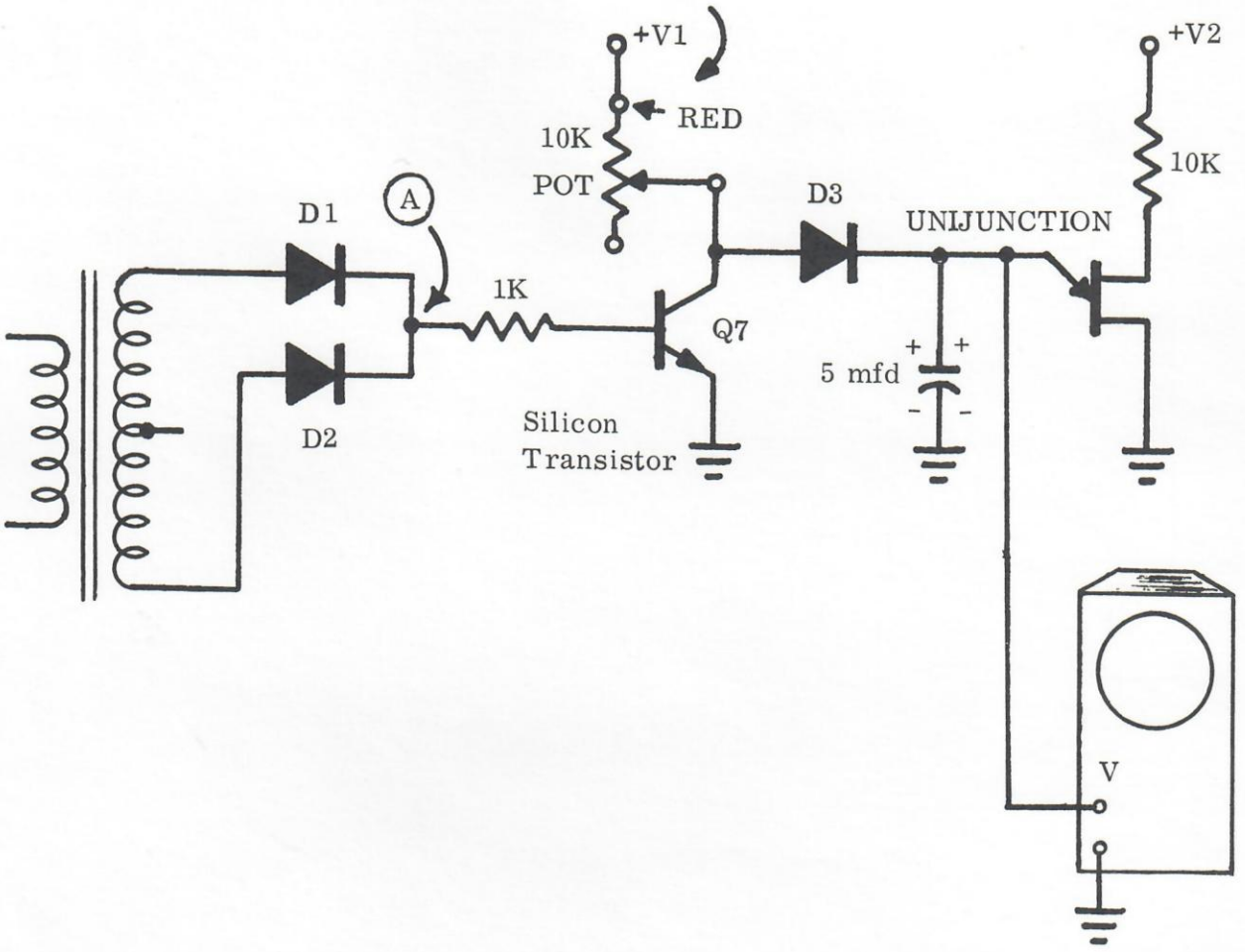


Figure 30 - 3 60 Hertz Staircase Generator

POT Position	# Steps	Period	Step Size	Voltage Sweep (volts)	Sweep Frequency
MIN					
MID					
MAX					

Position	# Steps	Period	Step Size	Voltage Range (volts)	Range Frequency
MIN					
MID					
MAX					

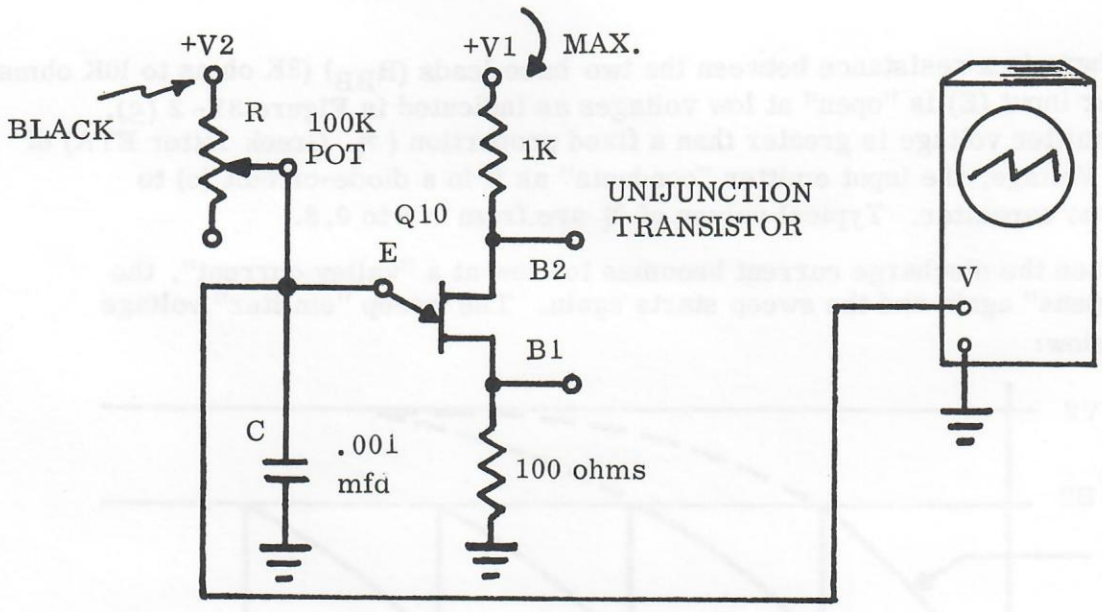


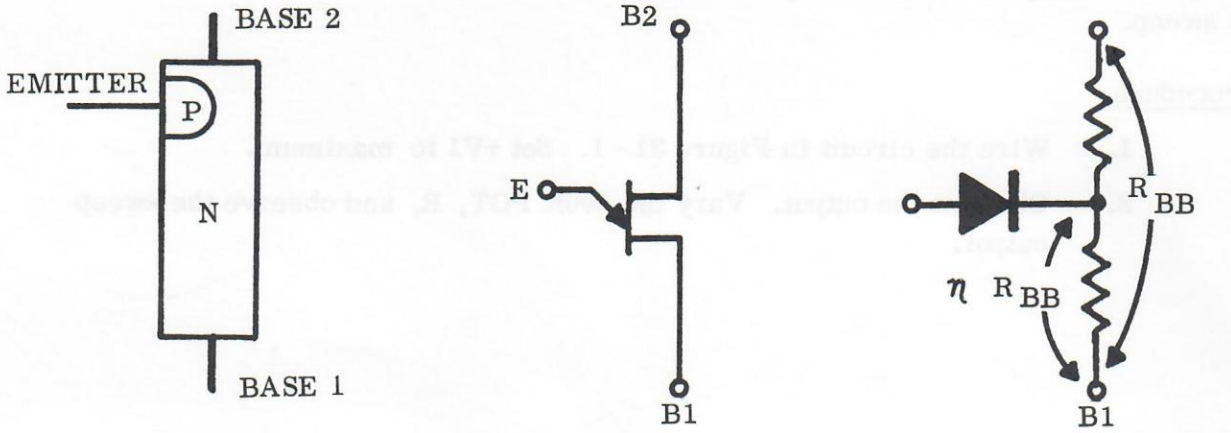
Figure 31-1 Uni-junction Sweep Circuit

Objective:

You will use an R - C Timing Circuit and a UNIJUNCTION TRANSISTOR as a SWEEP CIRCUIT.

Description:

The previous experiment used the Unijunction Transistor to "discharge" the capacitor in the Staircase Generator. The Unijunction consists of a Base material of N-Type Silicon with a single (uni) junction of R-type emitter as shown below:



(a) Construction (b) Symbol (c) Operation

Figure 31-2 Uni-junction Transistor

There is a resistance between the two base leads (R_{BB}) (3K ohms to 10K ohms). The Emitter input (E) is "open" at low voltages as indicated in Figure 31-2 (c). When the emitter voltage is greater than a fixed proportion (η Greek letter ETA) of the Base 2 Voltage, the input emitter "conducts" as if in a diode-circuit (c) to discharge the capacitor. Typical values of η are from 0.5 to 0.8.

When the discharge current becomes too low at a "valley current", the Emitter "opens" again and the sweep starts again. The sweep "emitter" voltage is shown below:

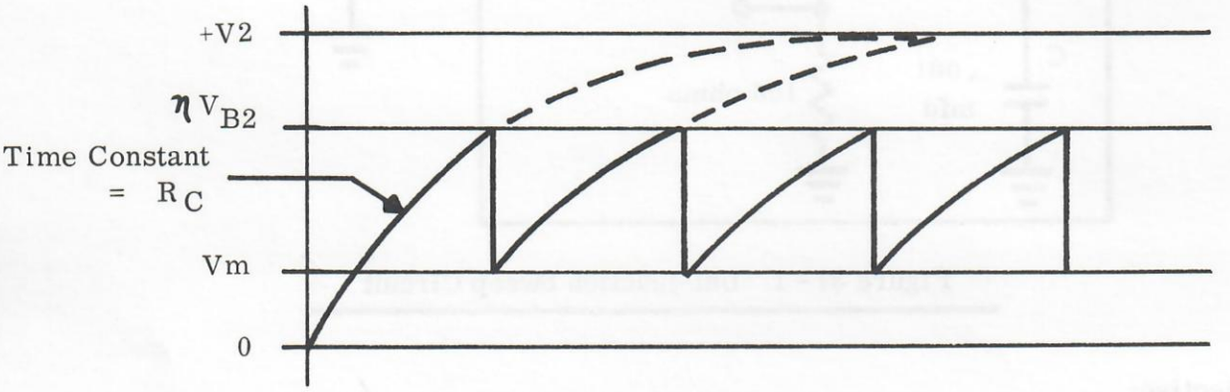


Figure 31-3 Unijunction Sweep Voltage

If the charging resistor, R, is too large, there will not be enough current to turn the transistor - ON. If the charging resistor, R, is too low, there will always be enough current to keep the emitter or transistor ON and there will be no sweep.

Procedure:

1. Wire the circuit in Figure 31-1. Set +V1 to maximum.
2. Observe the output. Vary the 100K POT, R, and observe the sweep output.

Sketch the sweep output below for R = 50K.

Record the Sweep Period, and the lower and upper voltage levels.

SWEEP VOLTAGE

3. Calculate the time constant:

$\tau = RC$

$\tau = (50\ \ 10^3)\ (.001\ 10^{-6})$

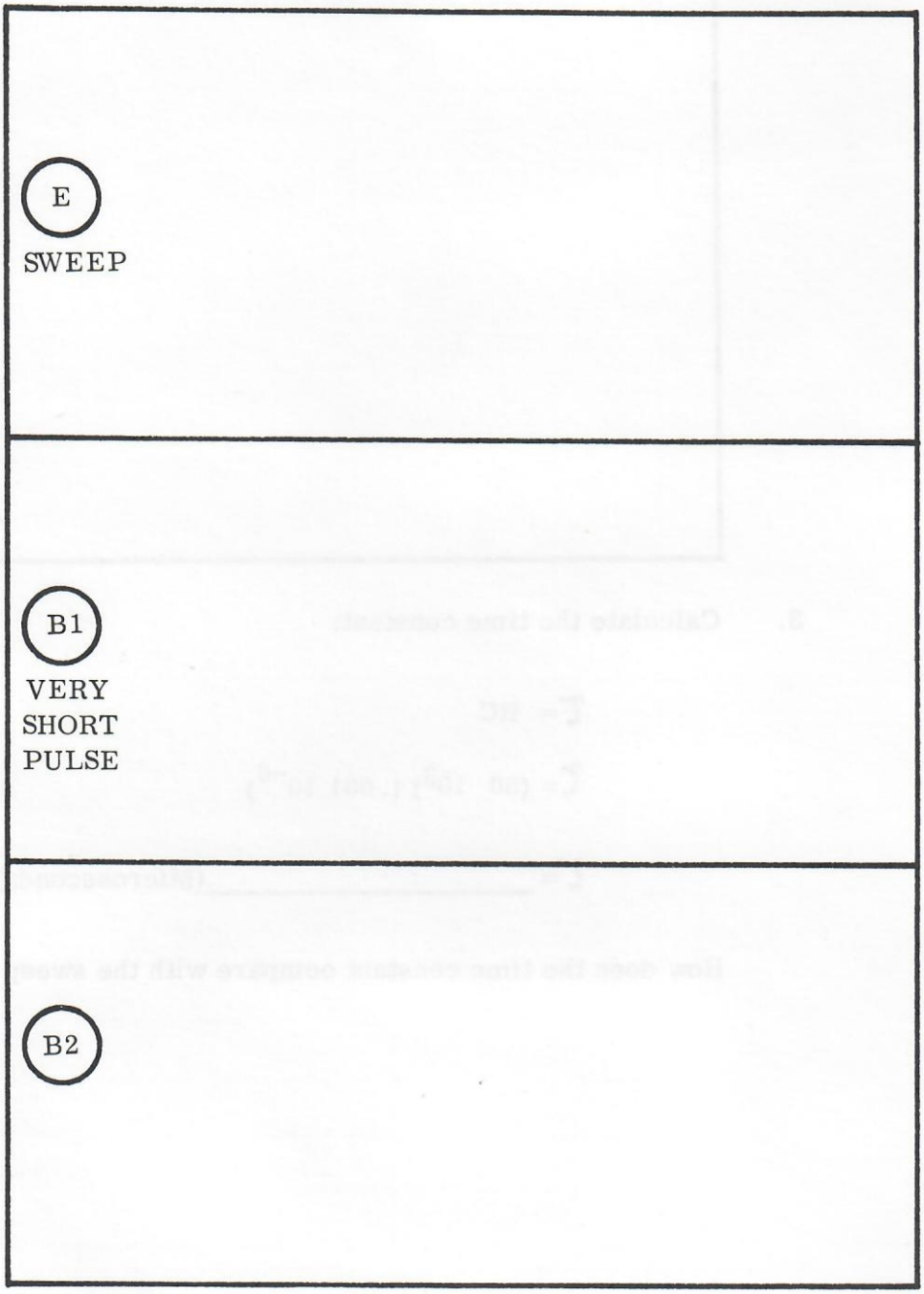
$\tau =$ _____ (Microseconds)

How does the time constant compare with the sweep period?

4. Set R = 100K

Plot the voltages at the emitter E and at bases B1 and B2"

WAVEFORMS



5. Adjust the 100K POT to the lowest resistance which will result in a sweep voltage. This is at the shortest period. Record the results below:

$R_{(LOWEST)}$ =
$PERIOD_{(LOWEST)}$ =

6. Replace the 100K POT with a 1 MEGOHM POT. Vary the POT Resistance and adjust R for the lowest frequency, or longest period; that is, the highest resistance. Record the results below:

$R_{(LARGEST)}$ =
$PERIOD_{(LARGEST)}$ =

7. Replace R with the 100K POT and set the POT at R = 50K.

Substitute various other capacitors and measure the Sweep Period. Enter the data below:

CAPACITANCE (for R = 50K)	SWEEP PERIOD
.001 mfd	
.01 mfd	
.25 mfd	
10 mfd	
100 mfd	
150 pfd	
C (open) (remove wires)	

8. Leave the R POT set at 50K. Insert C = 0.25 mfd.

Observe the output sweep waveform which results from the R - C timing "exponential" and is a "non-linear" waveform. A method of "linearizing' or "straightening" the sweep is by connecting the timing resistor R to a larger voltage. This is demonstrated by reducing the Unijunction voltage, +V1.

Reduce +V1 by rotating the power supply knob and observe the linear sweep. The period also decreases. Reduce +V1 to approximately 1/2 full value. Plot the new sweep voltage below:

LINEAR SWEEP VOLTAGE

Is the new sweep voltage more linear?

9. The linearity is measured by the "difference" between a "straight line" and the sweep as shown:

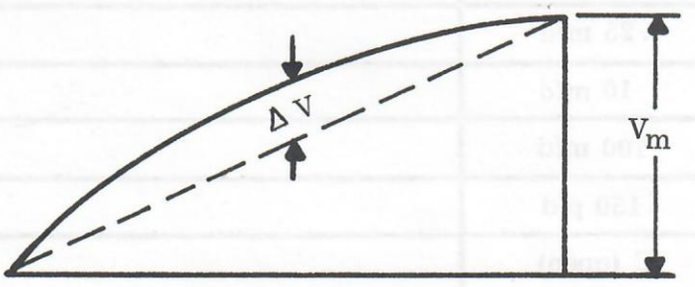


Figure 31 - 4 Linearity Measurement

The percentage of "non-linearity" is given by:

$$\text{Non-Linearity} = \frac{\Delta V}{V_m} \times 100\%$$

With +V1 set at maximum, use a sheet of paper on the oscilloscope face to act as the dashed-line in Figure 31-4, and read the value of ΔV. Then read V_m. Then calculate the non-linearity

Measure

ΔV =
V_m =

Calculate

Non-Linearity = $\frac{\Delta V}{Vm}$ x 100%
=

Ed-Lab | UNIJUNCTION PULSE GENERATOR | EXP. NO. 32 Page No. 1

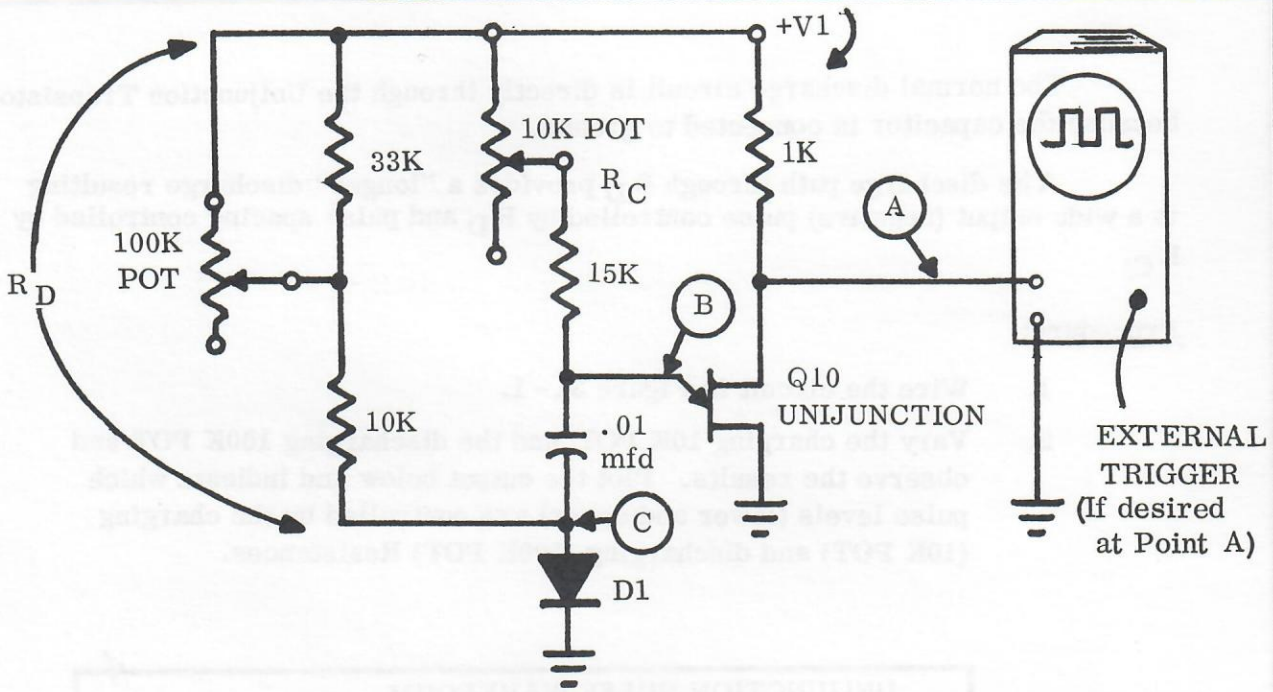


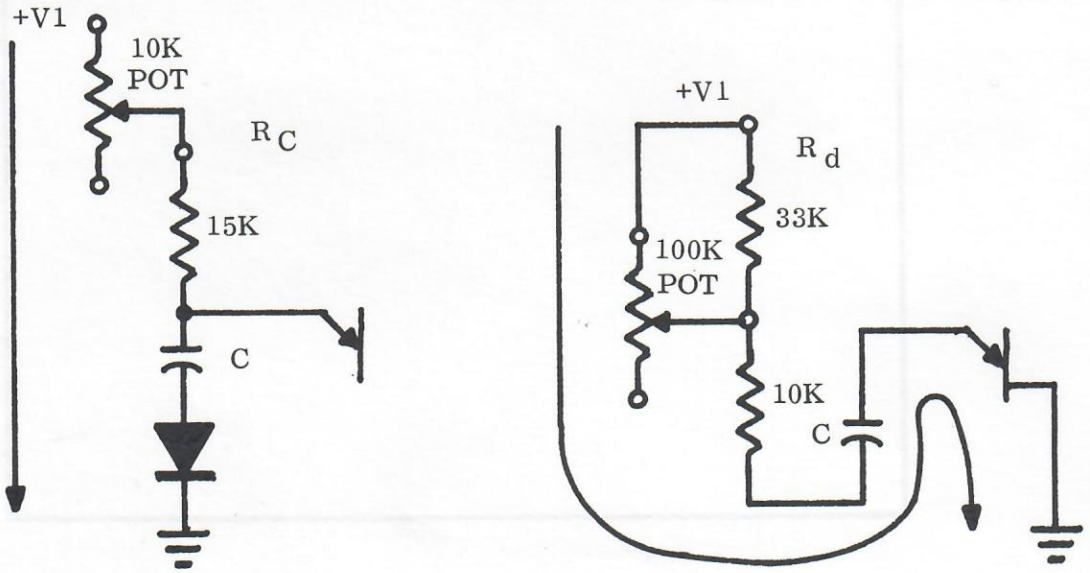
Figure 32-1 Unijunction Pulse Generator

Objective:

You will use a Unijunction Sweep Circuit with a DIODE and TWO RESISTORS to result in a PULSE GENERATOR.

Description:

The Diode provides different charge and discharge paths as shown below:



(a) Charging Circuit

(b) Discharging Circuit

Figure 32-2 Capacitor Charge Paths

The normal discharge circuit is directly through the Unijunction Transistor because the capacitor is connected to ground.

The discharge path through R_D provides a "longer" discharge resulting in a wide output (negative) pulse controlled by R_D and pulse spacing controlled by R_C.

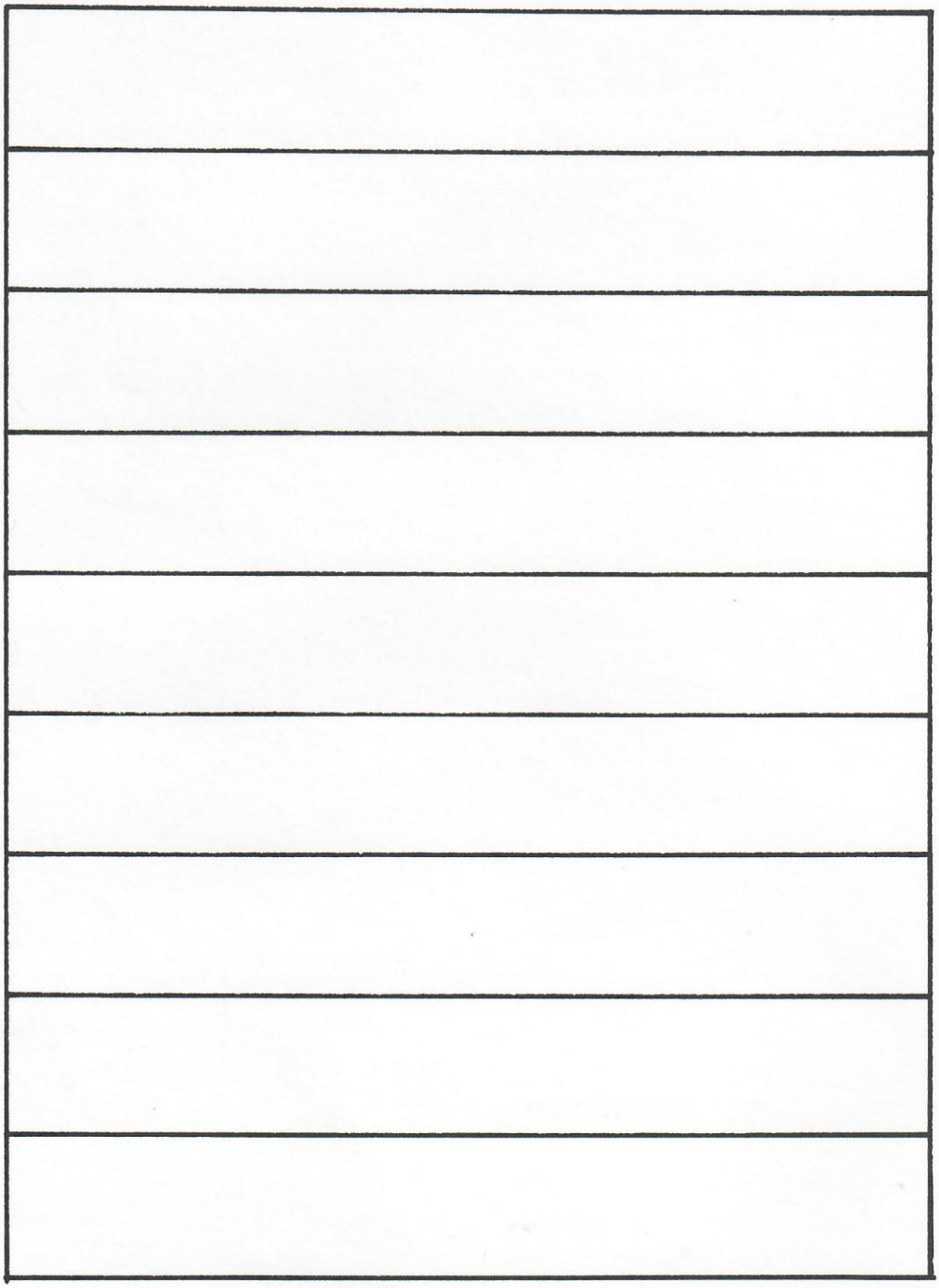
Procedure:

1. Wire the circuit in Figure 31 - 1.
2. Vary the charging 10K POT and the discharging 100K POT and observe the results. Plot the output below and indicate which pulse levels (lower and upper) are controlled by the charging (10K POT) and discharging (100K POT) Resistances.

UNIJUNCTION PULSE WAVEFORM

3. Set the 10K POT and 100K POT both to zero. Plot the waveforms at points A , B , and C all on the same graph below:

UNIJUNCTION WAVEFORMS



Ed-Lab | BOOTSTRAP SWEEP CIRCUIT | EXP. NO. 33 Page No. 1

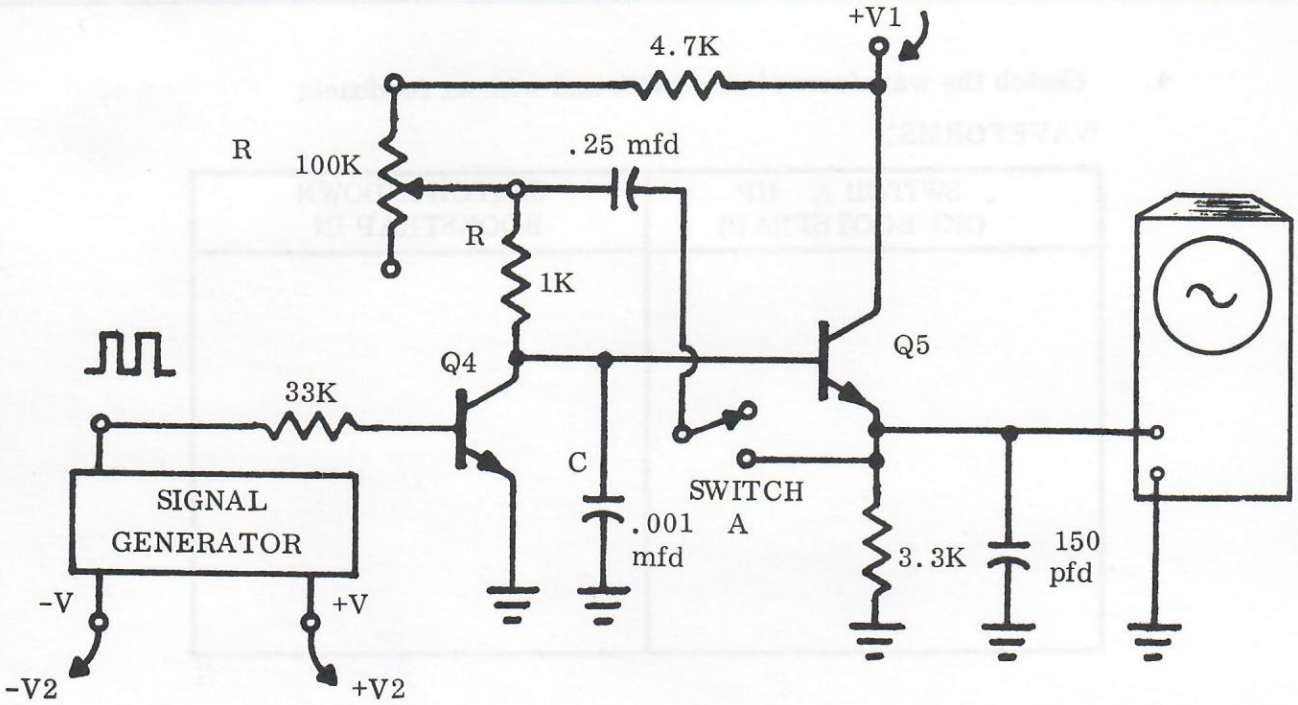


Figure 33 - 1 Bookstrap Sweep Circuit

Objective:

You will use a Transistor Squaring Circuit and an R - C NETWORK to generate a SWEEP VOLTAGE. Feedback is used in a BOOTSTRAP Circuit to make the sweep more LINEAR.

Description:

The Collector resistor, R (4.7K in series with the 100K POT and the 1K resistor) and the capacitor C (.001 mfd) form an R.C. Low Pass Sweep circuit. The Emitter Follower is just a BUFFER to prevent LOADING of the RC network. A feedback capacitor (0.25 mfd) connects the output sweep voltage to the sweep voltage source. The RC Sweep Voltage normally decreases in slope, but the "feedback" tends to keep the sweep increasing or linear. The output is holding the input up by its own "bootstraps". Switch A is used to control the feedback; IN and OUT.

Procedure:

1. Wire the circuit in Figure 33 - 1.
2. Keep switch A UP; No Feedback.
3. Set the 100K pot at ZERO ohms.

4. Sketch the waveforms below with and without feedback:

WAVEFORMS:

SWITCH A UP (NO BOOTSTRAP)	SWITCH A DOWN BOOKSTRAP IN

5. With the Bookstrap IN (Switch A DOWN), adjust the 100K POT for a full sweep without a flat-top. Sketch the waveform below: Estimate the setting of the 100K POT resistance.

WAVEFORMS:

BOOTSTRAP SWEEP R_{pot} = _____

6. Measure the sweep RATE (volts per second).

RATE =

7. Modify the input to circuit for a repetitive sweep, as shown below by removing the 33K resistor and adding the 330 pfd CAP and the 100 ohm resistor PULSE COMPRESSOR.

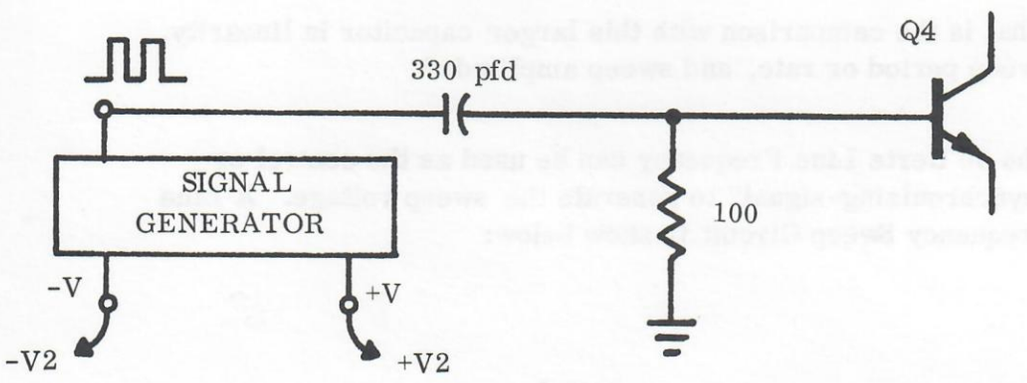


Figure 33 - 2 Input Modification

The result is a continuous sweep with a short "reset or retrace time".

8. Sketch the result below. Measure the sweeptime and amplitude.

WAVEFORM:

Sweep Time = _____ Sweep Amplitude = _____

9. Calculate the SWEEP REPETITION RATE in SWEEPS PER SECOND.

SWEEP REPETITION RATE =

10. Substitute a 0.01 mfd capacitor for the .001 mfd timing capacitor.

What is the camparison with this larger capacitor in linearity, sweep period or rate, and sweep amplitude?

11. The 60 Hertz Line Frequency can be used as the control or "synchronizing-signal" to generate the sweep voltage. A Line Frequency Sweep Circuit is show below:

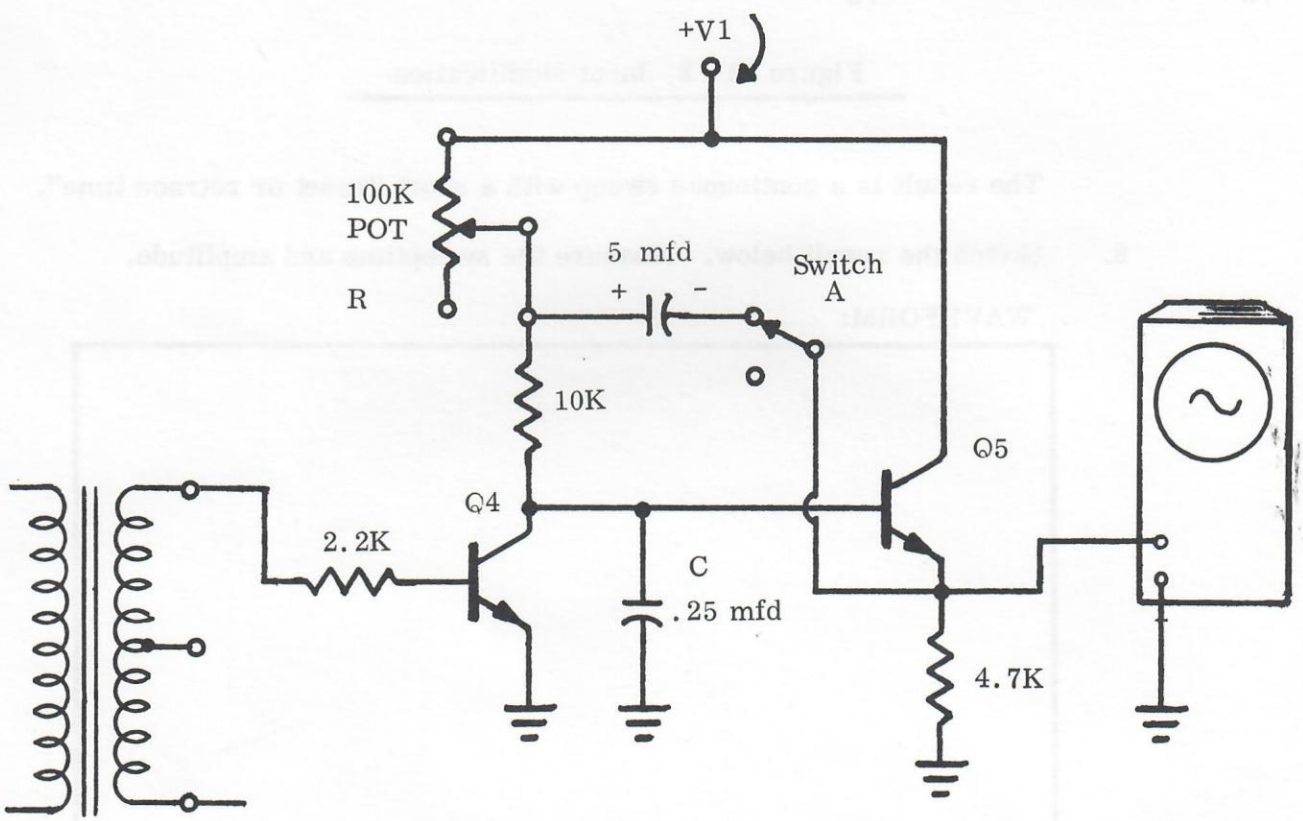
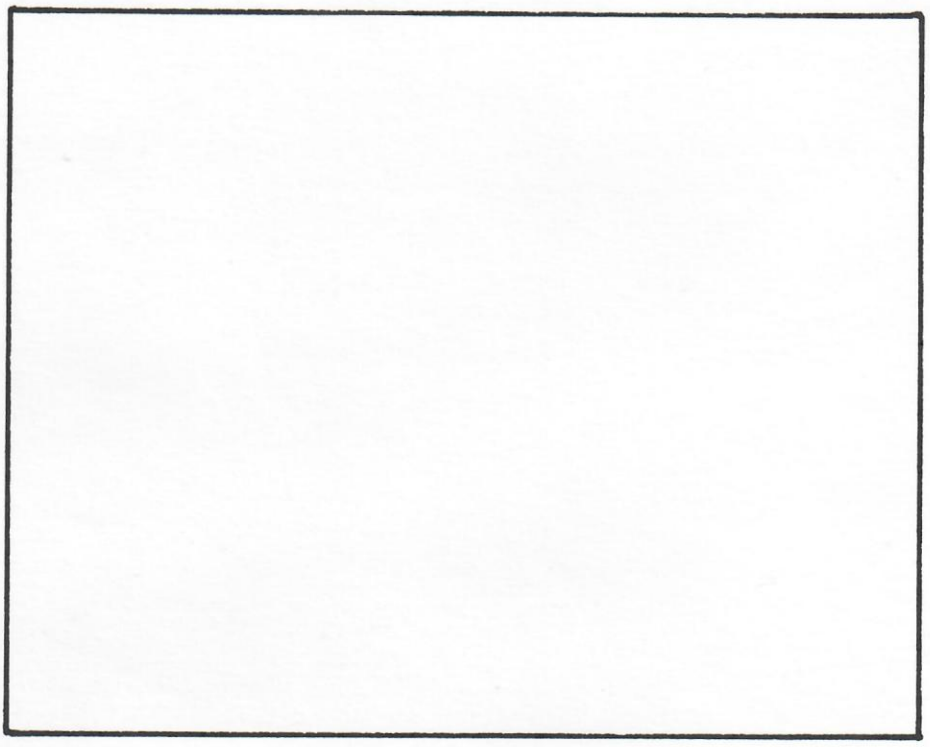


Figure 33-3 Line Frequency Bootstrap Sweep

12. Wire the Line Frequency Sweep from Figure 33 - 3.

Plot the output Waveshape below:

WAVESHAPE:



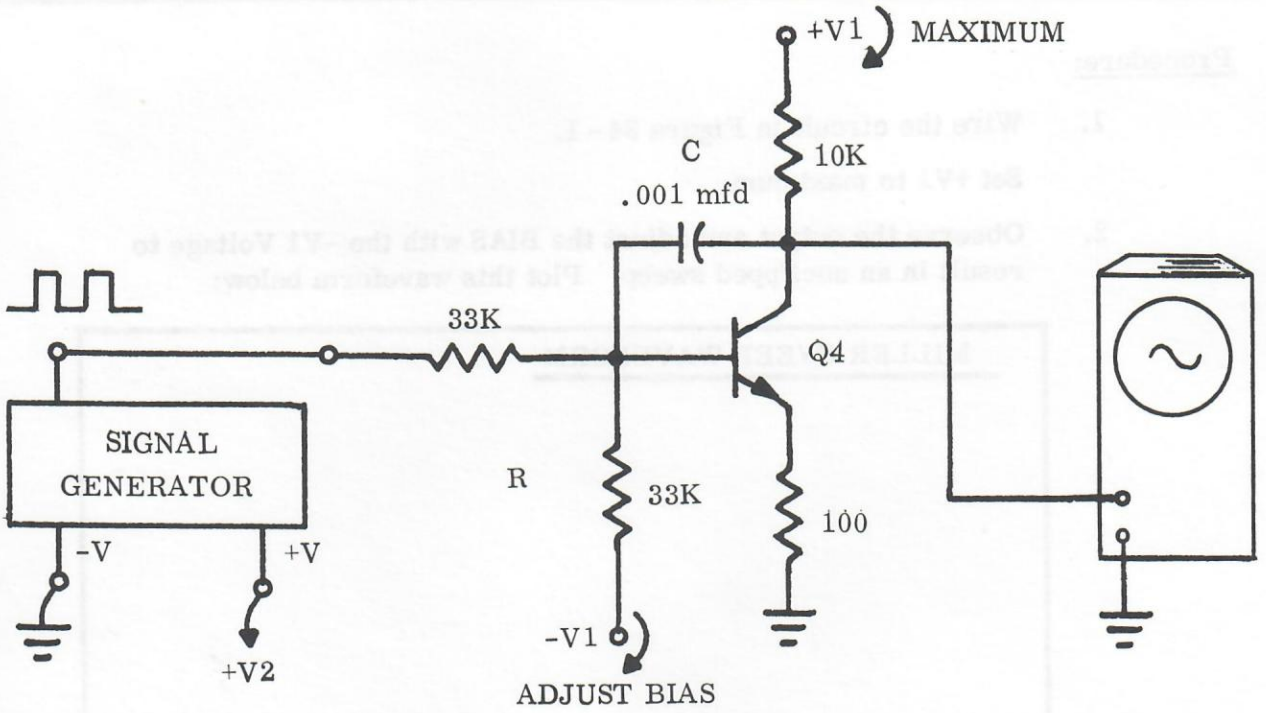


Figure 34 - 1 Miller Sweep

Objective:

You will use an AMPLIFIER with a RESISTOR input and a CAPACITOR feedback as an "ideal" R - C INTEGRATOR CIRCUIT or "MILLER" SWEEP CIRCUIT.

Description:

A High-Gain Amplifier with a capacitor-feedback results in an Integrator Circuit.

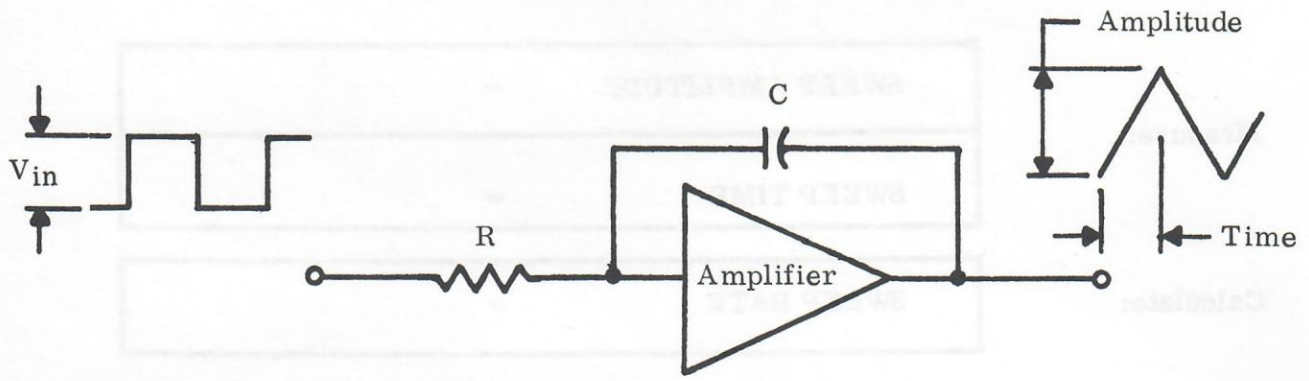


Figure 34 - 2 Integrator

Procedure:

1. Wire the circuit in Figure 34 - 1.

   Set +V1 to maximum.

2. Observe the output and adjust the BIAS with the -V1 Voltage to result in an unclipped sweep. Plot this waveform below:

MILLER SWEEP WAVEFORM

Measure the Sweep Amplitude and the Sweep Time. Calculate the Sweep Rate in Volts per Microsecond:

Measure:

SWEEP AMPLITUDE	=
SWEEP TIME	=

Calculate:

SWEEP RATE	=

3. An OPERATIONAL AMPLIFIER (OP-AMP) is a very high gain amplifier which is used for an Integrator or Miller Sweep in the circuit shown below:

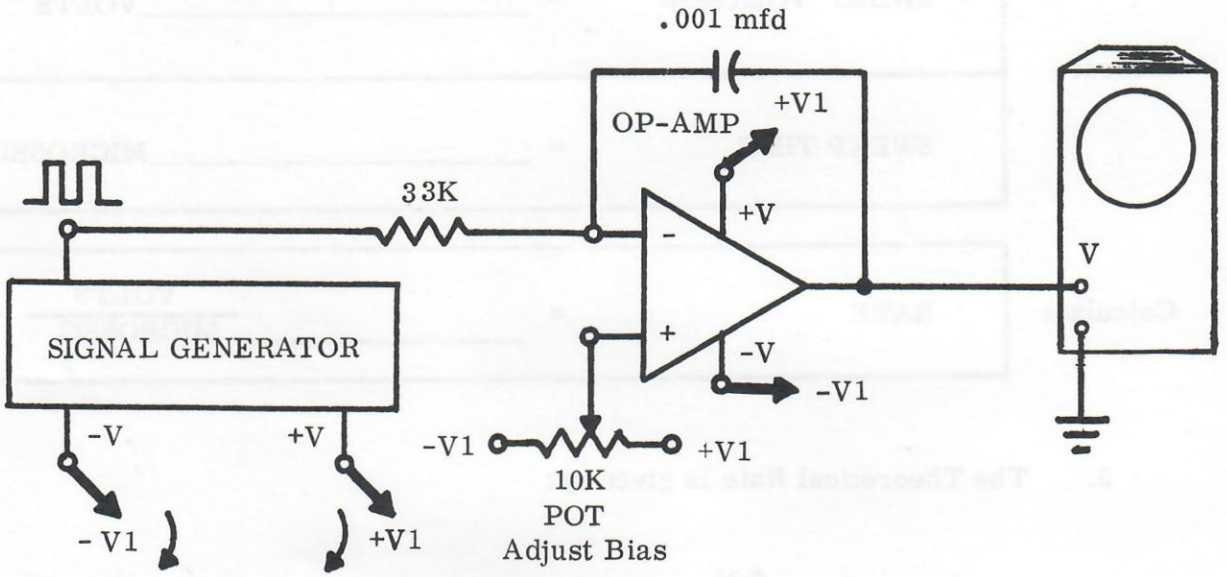


Figure #4 - 2 OP-AMP Miller Sweep

4. Wire the above circuit in Figure 34 - 2. Adjust the 10K POT for a good output waveform. Plot the waveform below:

OP-AMP SWEEP WAVEFORM

Measure the Sweep Rate in Volts per Microsecond:

Measure

SWEEP VOLTAGE = _____ VOLTS	
SWEEP TIME = _____ MICROSEC	

Calculate

RATE = _____ $\frac{\text{VOLTS}}{\text{MICROSEC}}$	

5. The Theoretical Rate is given by:

$$\text{Rate} = \frac{\Delta V}{RC}$$

Where: ΔV = Input Voltage (offset from - INPUT) (Approx. 7 volts)

$R = 33\ 10^{-3}$ ohms

$C = .001\ 10^{-6}$ farads

$$\text{Rate} = \frac{\Delta V}{RC} = \frac{7}{(33\ \ 10^{3})\ (.001\ \ 10^{-6})}$$

$$= \frac{7}{(33)\ 10^{-6}} \qquad \frac{\text{VOLTS}}{\text{SEC}}$$

$$= \frac{7}{33} \qquad \frac{\text{VOLTS}}{\text{MICROSEC}}$$

Calculate:

Rate = _____ $\frac{\text{VOLTS}}{\text{MICROSEC}}$	

How does the measured rate compare with the theoretical rate?

Ed-Lab | SCHMITT TRIGGER | EXP. NO. 35 Page No. 1

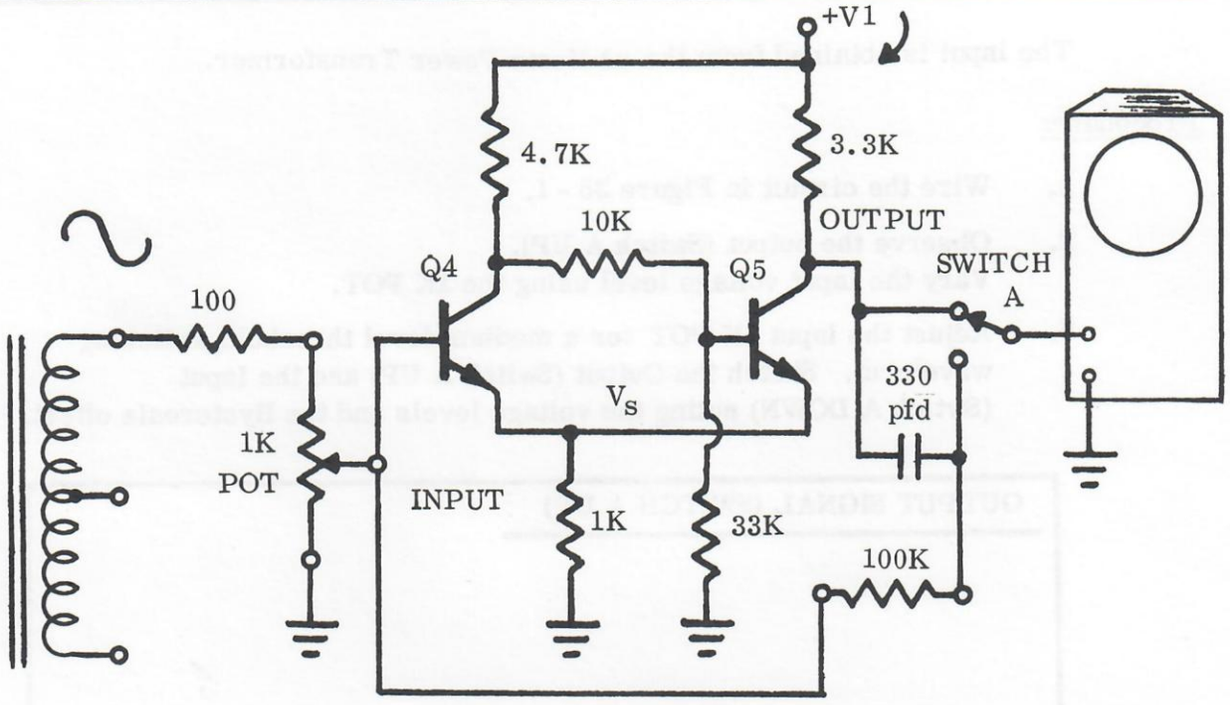


Figure 35 - 1 Schmitt Trigger

Objective:

You will test a SCHMITT TRIGGER Level Sensing Circuit and measure the THRESHOLD LEVEL and the HYSTERESIS.

Description:

The Schmitt Trigger Circuit shown in Figure 35 - 1 is similar to the "Emitter Coupled Multivibrator" with a Direct Coupled Input to the Base of Transistor Q5.

When the INPUT voltage is low, transistor Q5 is ON and the Emitter Voltage (V_S) is given by the voltage divider ratio between the 3.3K Collector Resistor and the 1K Emitter Resistor and is approximately 2 volts. When the INPUT voltage reaches a "threshold" greater than the emitter voltage, V_S, Transistor Q4 is turned ON resulting in a lower Q4 collector voltage which turns Q5 OFF. The new, V_S, calculated by the voltage divider between the 4.7K collector resistor and the 1K emitter resistor is lower because the collector resistor is higher. The INPUT voltage which switches the input transistor Q4 "back-OFF" is thus lower and the difference between these two voltages is called the HYSTERESIS.

Switch A is used to observe the Input and the Output. The 330 pfd and 100K resistor "couples" a sharp edge from output waveform to the input 60 Hertz Signal so that we can observe the input together with an output switching "time-marker".

The input is obtained from the 60 Hertz Power Transformer.

Procedure:

1. Wire the circuit in Figure 35 - 1.
2. Observe the output (Switch A UP).
   Vary the input voltage level using the 1K POT.
3. Adjust the input 1K POT for a medium level threshold switching waveform. Sketch the Output (Switch A UP) and the Input (Swtich A DOWN) noting the voltage levels and the Hysteresis offset.

OUTPUT SIGNAL (SWITCH A UP)

INPUT SIGNAL (SWITCH A DOWN)

"Positive Going" Switching Level = _____ volts

Hysteresis = _____ volts

Ed-Lab | INDUCTIVE DRIVER | EXP. NO. 36 Page No. 1

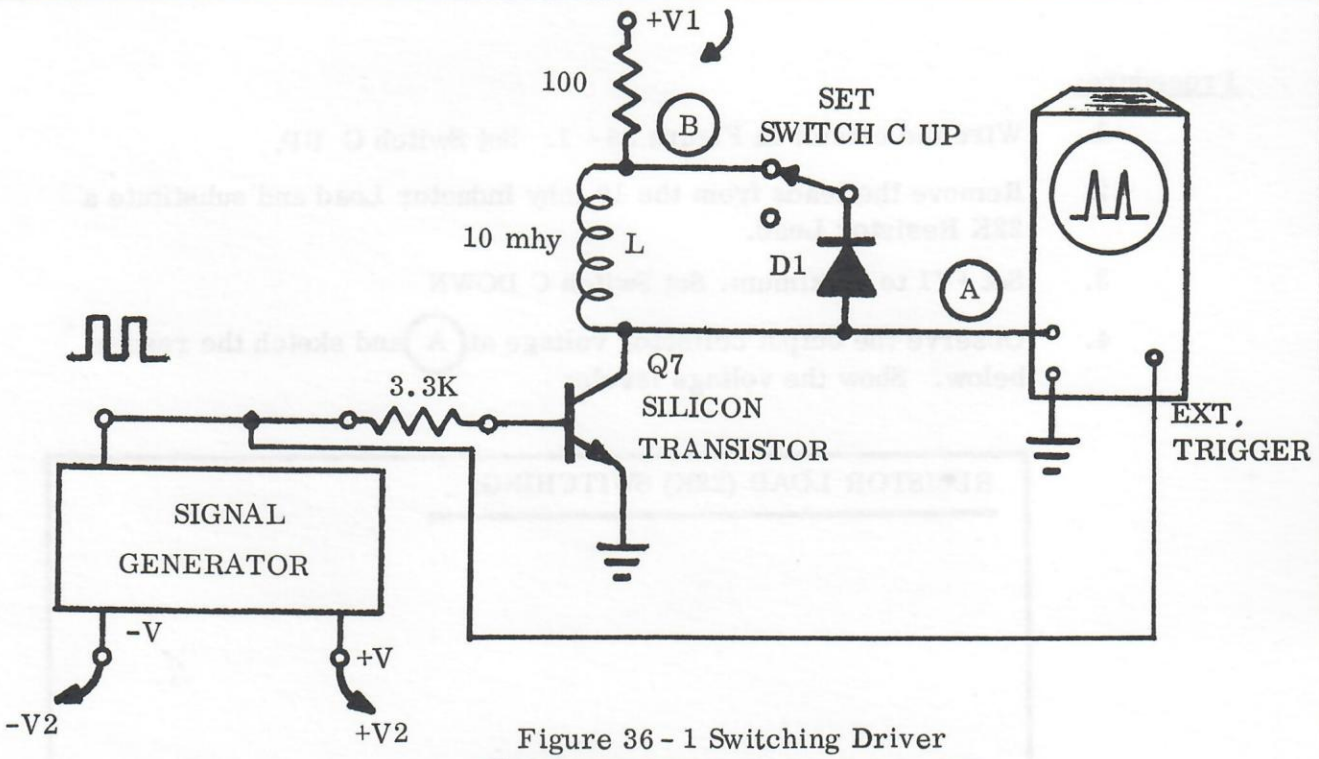


Figure 36 - 1 Switching Driver

Objective:

You will drive a Transistor Switch with a pulse and observe the output when using an INDUCTANCE as the LOAD. You will observe the "high reverse" voltage or "inductive-kick" obtained when driving an Inductor such as a Relay Coil, and you will eliminate these undesired spikes using a DIODE.

Description:

When current flow (ΔI) in an INDUCTOR (L) is stopped or reduced in a time duration (ΔT), a reverse Voltage (V) is "induced" with an amplitude given by the equation:

$$V = L \frac{\Delta I}{\Delta T}$$

When the current is cut-off in a short time (ΔT), a very large voltage (V) can be induced, and this large voltage can damage or burn-out transistors or other circuit components. A reverse diode, D1, provides a current "discharge" patch to eliminate this voltage. The Diode is in the circuit with Switch C-UP. The series 100 ohm resistor allows us to measure the collector or inductor current.

Procedure:

1. Wire the circuit in Figure 36 - 1. Set Switch C UP.
2. Remove the leads from the 10 mhy Inductor Load and substitute a 22K Resistor Load.
3. Set +V1 to maximum. Set Switch C DOWN
4. Observe the output collector voltage at (A) and sketch the results below. Show the voltage levels:

RESISTOR LOAD (22K) SWITCHING:

BASE LEVEL = _____ volts

PULSE AMPLITUDE = _____ volts

5. Replace the 22K LOAD resistor with the 10 mhy INDUCTOR LOAD. Keep Switch C DOWN to remove the DIODE from the circuit.
6. Observe the output on the oscilloscope and sketch the waveshape below: The current switching results in a large inductive "spike" or "kick". Be sure to adjust the oscilloscope to be able to see the full amplitude of the pulse.

INDUCTIVE KICK (L = 10 mhy) (Silicon Transistor)

FIRST-SPIKE AMPLITUDE = _____ VOLTS

7. The spike amplitude is not really the full inductive voltage; the top of the spike is clipped because the transistor "breaks down" due to the high voltage. This can be illustrated by reducing the +V1 voltage and observing the effect on the spike.

   Reduce the supply voltage +V1 to result in a spike below breakdown. Sketch the output (A) below.

   Also sketch the waveform at (B) to measure the current, based on the voltage pulse change or amplitude E across the 100 ohm series resistor. Measure the current stopping time, as the rise time for the positive-going pulse.

   Also measure the supply voltage, +V1, using the oscilloscope.

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INDUCTIVE KICK WAVESHAPES

(Reduce +V1 to PREVENT CLIPPING)

Ⓐ OUTPUT (VOLTAGE)

"KICK" AMPLITUDE (V) = _____

SILICON BREAKDOWN VOLTAGE = _____

Ⓑ OUTPUT (CURRENT) (100 OHM Resistor Voltage)

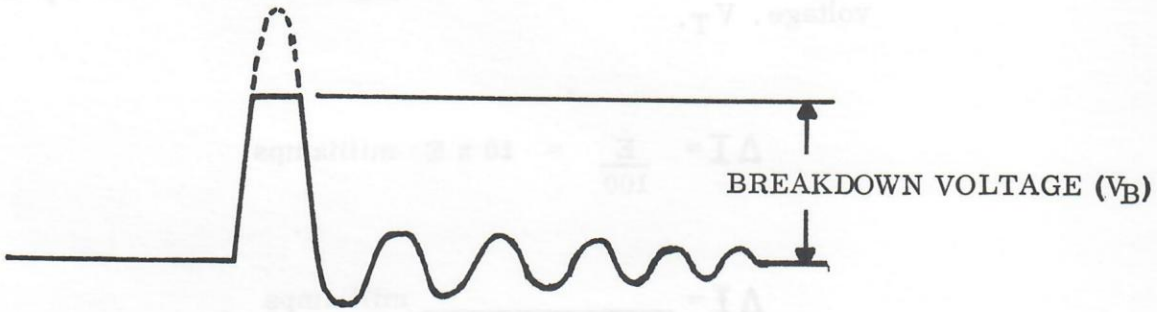
CURRENT-OFF (Rise-Time) (ΔT) = _____ microsecs.

PULSE AMPLITUDE (E) = _____ volts.

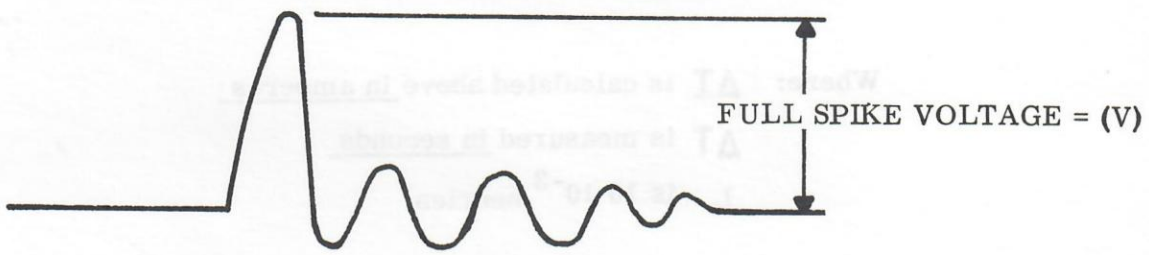
SUPPLY VOLTAGE (Use oscilloscope)

+V1 VOLTAGE = _____ volts.

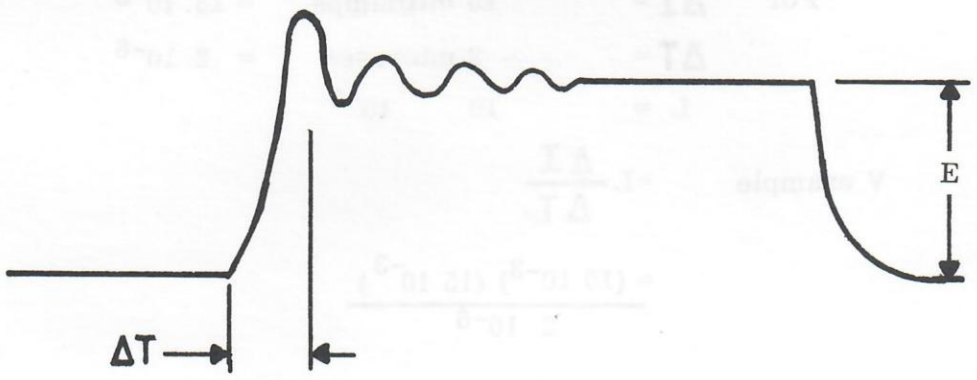
Typical pulses are:



(a) +V1 at Full Setting



(b) Reduced +V1 to Prevent Breakdown



(c) Current Waveform (100 ohm Resistor)

Figure 36 - 2 Typical Waveforms

8. Calculate the change in current (ΔI) and the theoretical pulse voltage, V_T,

$$\Delta I = \frac{E}{100} = 10 \times E \text{ milliamps}$$

$\Delta I =$ _____ milliamps

$$V_T = L \frac{\Delta I}{\Delta T}$$

Where: ΔI is calculated above in amperes

ΔT is measured in seconds

L is 10 10^{-3} henries.

A typical calculation is

For $\Delta I =$ 15 milliamps $= 15.10^{-3}$

$\Delta T =$ 2 microsec $= 2.10^{-6}$

L = 10 10^{-3}

V example $= L \frac{\Delta I}{\Delta T}$

$$= \frac{(10\ 10^{-3})\ (15\ 10^{-3})}{2\ 10^{-6}}$$

$$= \frac{150}{2}$$

V example = 75 volts

Calculate the spike voltage from your measurements:

$$\Delta I = \frac{E}{100}$$

$\Delta I =$

$$V_T = L \frac{\Delta I}{\Delta T}$$

$V_T =$

How does the calculated (V_T) and the measured (V) compare?

10. Observe the effect of the DIODE with Switch A UP and DOWN. Sketch the results below: Indicate the voltage levels. Set +V1 at maximum

WAVEFORMS

(A) SPIKE (SWITCH C DOWN)	(A) SWITCH C UP
(NO DIODE)	(DIODE PROTECTION)

Ed-Lab | BLOCKING OSCILLATOR | EXP. NO. 37 Page No. 1

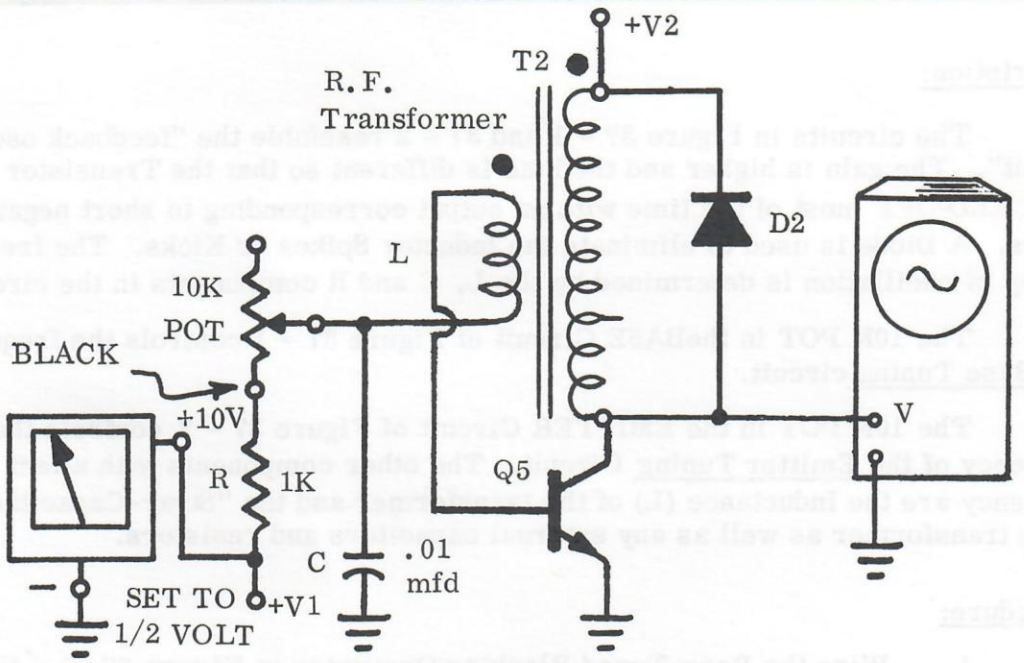


Figure 37 - 1 Base-Tuned Blocking Oscillator

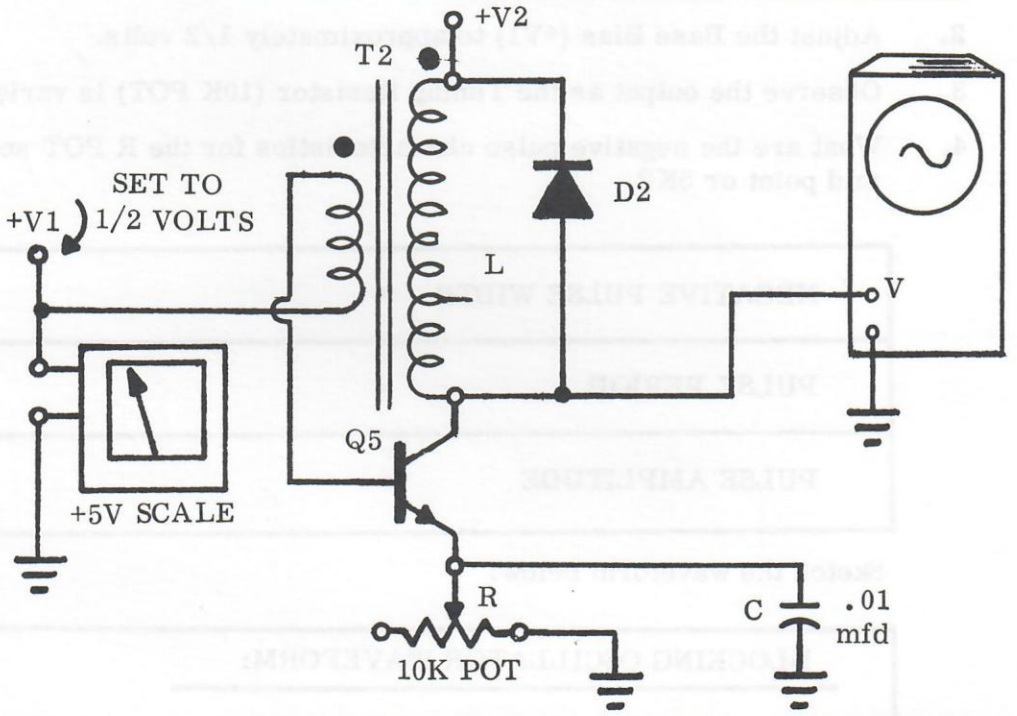


Figure 37 - 2 Emitter Tuned Blocking Oscillator

Objective:

You will use a high frequency "Pulse Transformer" in a feedback circuit as a Pulse Generator called a Blocking Oscillator.

Description:

The circuits in Figure 37 - 1 and 37 - 2 resemble the "feedback oscillator circuit". The gain is higher and the bias is different so that the Transistor is BLOCKED-OFF most of the time with an output corresponding to short negative pulses. A Diode is used to eliminate the Inductor Spikes or Kicks. The frequency of oscillation is determined by the L, C and R components in the circuit.

The 10K POT in theBASE Circuit of Figure 37 - 1 controls the frequency in a Base Tuning circuit.

The 10K POT in the EMITTER Circuit of Figure 37 - 2 controls the frequency of the Emitter Tuning Circuit. The other components with affect frequency are the Inductance (L) of the transformer and the "Stray-Capacitance" of the transformer as well as any external capacitors and resistors.

Procedure:

1. Wire the Base-Tuned Blocking Oscillator in Figure 37 - 1. Use the RF Transformer T2.
2. Adjust the Base Bias (+V1) to approximately 1/2 volts.
3. Observe the output as the Tuning Resistor (10K POT) is varied.
4. What are the negative pulse characteristics for the R POT set at mid point or 5K?

NEGATIVE PULSE WIDTH	=
PULSE PERIOD	=
PULSE AMPLITUDE	=

Sketch the waveform below:

BLOCKING OSCILLATOR WAVEFORM:

5. What are the pulse period or spacing (in microseconds: μsec) and the pulse widths for minimum and maximum settings of the R POT?

	MIN R POT	MAX R POT
PERIOD (μ sec)		
PULSE WIDTH (μsec)		

Observe that the transistor is ON for only a short period of time so that only a small amount of power is used in the circuit. Does varying R affect the period or width or both?

6. Substitute a .25 mfd capacitor and then a 1 mfd capacitor and then a .001 mfd capacitor for a full setting of the R = 10K POT. plus the series 1K resistors.

Record the Pulse Period or Pulse Width or Spacing below:

BASE-TUNED BLOCKING OSCILLATOR

Capacitance (set R = 10K	Pulse Period	Pulse Width
.01 mfd		
.001 mfd		
.25 mfd		
1 mfd		

7. Remove all wires and wire the circuit in Figure 37 - 2 for the Emitter-Tuned Blocking Oscillator. Set the +V1 voltage to 1/2 volts.

8. Vary the 10K Tuning POT and observe the results. Measure and record the Pulse width and the Maximum and Minimum Period for two different capacitors.

EMITTER-TUNED BLOCKING OSCILLATOR

CAPACITOR	.01 mfd	.25 mfd
PULSE WIDTH		
MAXIMUM PERIOD		
MINIMUM PERIOD		

Ed-Lab	DIODE LOGIC GATES: AND - OR	EXP. NO. 38 Page No. 1

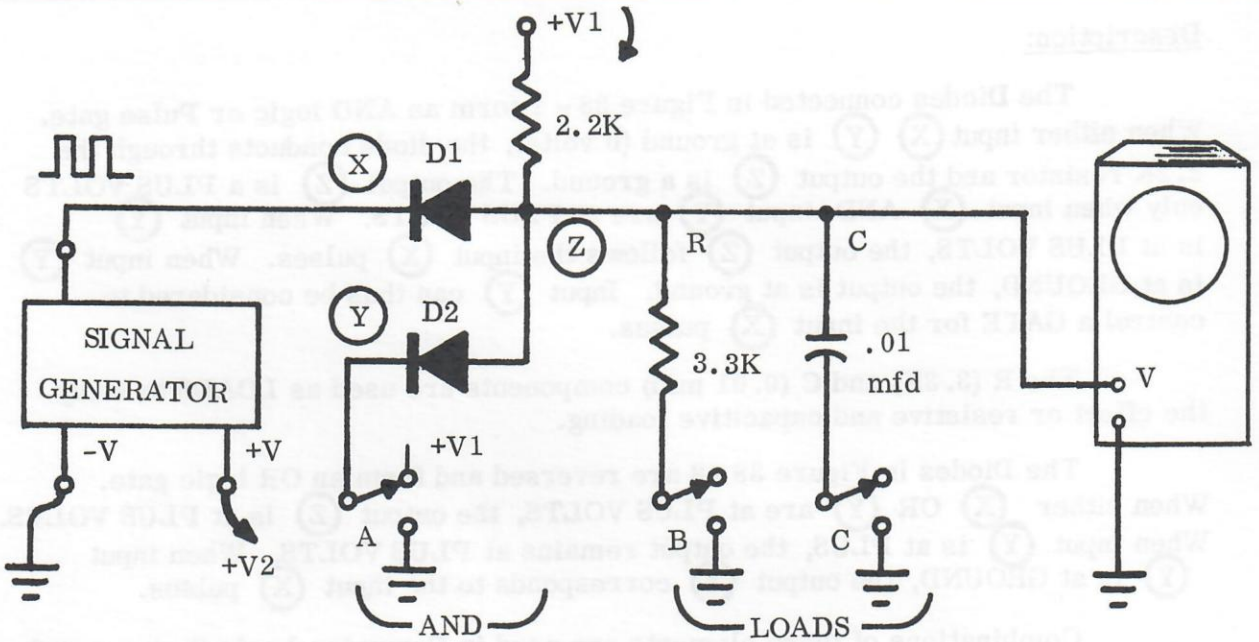


Figure 38 - 1 Diode Logic AND

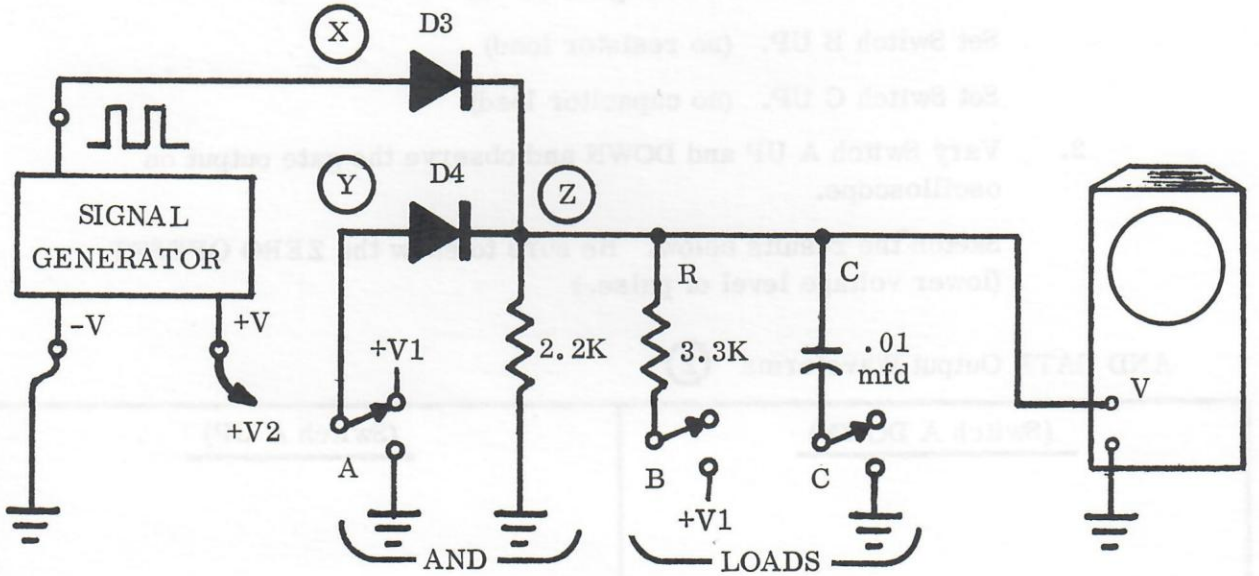


Figure 38 - 2 Diode Logic OR

Objective:

You will use DIODE-RESISTOR Circuits as Pulse Gate in AND and OR circuits.

Description:

The Diodes connected in Figure 38 - 1 form an AND logic or Pulse gate. When either input (X) (Y) is at ground (0 volts), the diode conducts through the 2.2K resistor and the output (Z) is a ground. The output (Z) is a PLUS VOLTS only when input (X) AND input (Y) are at PLUS VOLTS. When input (Y) is at PLUS VOLTS, the output (Z) follows the input (X) pulses. When input (Y) is at GROUND, the output is at ground. Input (Y) can thus be considered to control a GATE for the input (X) pulses.

The R (3.3K) and C (0.01 mfd) components are used as LOADS to study the effect or resistive and capacitive loading.

The Diodes in Figure 38 - 2 are reversed and form an OR logic gate. When either (X) OR (Y) are at PLUS VOLTS, the output (Z) is at PLUS VOLTS. When input (Y) is at PLUS, the output remains at PLUS VOLTS. When input (Y) is at GROUND, the output (Z) corresponds to the input (X) pulses.

Combinations of these elements are used in Computer Logic Systems and in Pulse Gating or Pulse Processing Systems.

Procedure:

1. Wire the AND ciruit in Figure 38 - 1.

   Set Switch B UP. (no resistor load)

   Set Switch C UP. (no capacitor load)

2. Vary Switch A UP and DOWN and observe the gate output on oscilloscope.

   Sketch the results below. Be sure to show the ZERO OFFSET (lower voltage level of pulse.)

AND GATE Output Waveforms (Z)

(Switch A DOWN)	(Switch A UP)
	OFFSET LEVEL = _____ volts

3. Observe the effects of Resistor and Capacitor Loading.

Keep Switch A UP to allow pulses to be gated to the output.

The effects of loading are the same as with the Transistor Switching Circuit.

Set Switch B DOWN and then Switch C DOWN and sketch the results below:

DIODE AND GATE Loading Waveforms

Switch A UP Switch B UP Switch C UP	NO LOAD Pulse Amplitude = _____ volts
Switch A UP Switch B DOWN Switch C UP	RESISTOR LOAD Pulse Amplitude= _____ volts
Switch A UP Switch B UP Switch C DOWN	CAPACITOR LOAD Rise Time = _____ volts

4. Remove all previous wires and wire the DIODE OR GATE in Figure 38 - 2. Sketch the Output Waveforms below:

DIODE OR GATE Loading Waveforms

Switch A UP Switch B UP Switch C UP	GATE OFF Voltage Level = _____ volts
Switch A DOWN Switch B UP Switch C UP	GATE ON Amplitude = _____ volts Zero Pulse Level = _____ volts
Switch A DOWN Switch B DOWN Switch C UP	RESISTOR LOAD Amplitude = _____ volts Zero Pulse Level = _____ volts
Switch A DOWN Switch B UP Switch C DOWN	CAPACITOR LOAD Rise Time = _____

The effect of capacitor loading is to increase the rise and fall time. The resistor load is returned to a POSITIVE Voltage as it would be if the OR gate output were connected to an AND gate input. The Low Level of the Pulse shifts too much with a resistor load to permit such a load to be used with the OR Gate. A Transistor Amplifier must generally be used after a DIODE OR GATE Circuit, before connecting such a circuit to an AND gate. An AND gate output can however be connected to an OR gate input.

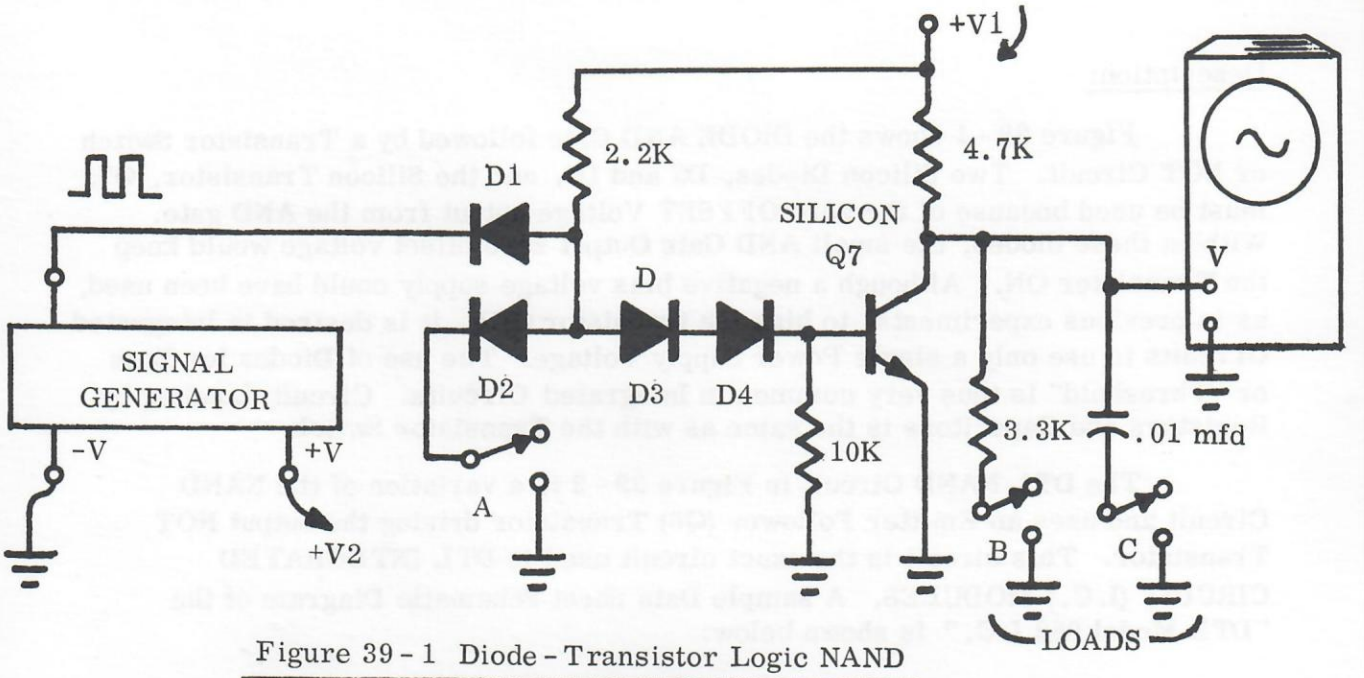


Figure 39 - 1 Diode - Transistor Logic NAND

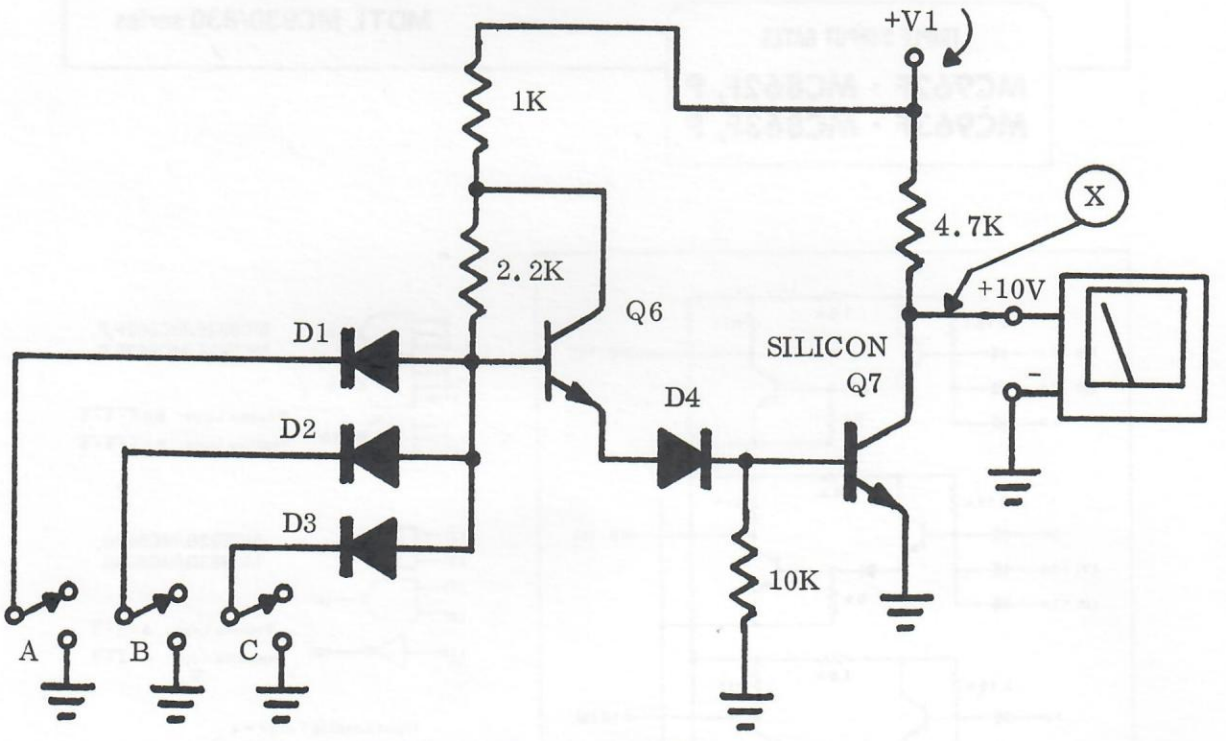


Figure 39 - 2 DTL Integrated Circuit NAND

Objective:

You will combine the DIODE LOGIC AND with a Transistor Switch or Inverter or NOT Circuit to result in a NOT-AND Digital Logic Circuit called a N-AND.

Description:

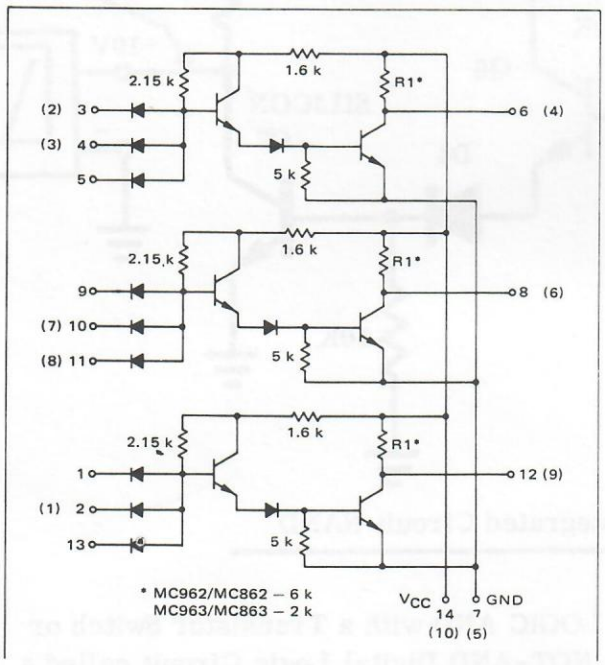
Figure 39 - 1 shows the DIODE AND Gate followed by a Transistor Switch or NOT Circuit. Two Silicon Diodes, D3 and D4, and the Silicon Transistor, Q7, must be used because of the zero OFFSET Voltage output from the AND gate. Without these diodes, the small AND Gate Output zero offset voltage would keep the Transistor ON. Although a negative bias voltage supply could have been used, as in previous experiments, to bias the transistor OFF, it is desired in Integrated Circuits to use only a single Power Supply Voltage. The use of Diodes for Bias or "Threshold" is thus very common in Integrated Circuits. Circuit Loading by Resistors and Capacitors is the same as with the Transistor Switch.

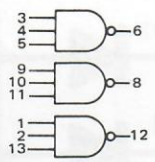
The DTL NAND Circuit in Figure 39 - 2 is a variation of the NAND Circuit and uses an Emitter Follower (Q6) Transistor driving the output NOT Transistor. This circuit is the exact circuit used in DTL INTEGRATED CIRCUIT (I.C.) MODULES. A sample Data Sheet Schematic Diagram of the "DTL Model 862 I.C." is shown below:

MDTL MC930/830 series

TRIPLE 3-INPUT GATES

MC962F · MC862F, P
MC963F · MC863F, P

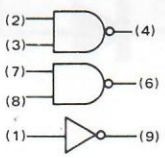




MC962F/MC862F,P
MC963F/MC863F,P

Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Negative Logic: $6 = \overline{3 + 4 + 5}$



MC962G/MC862G
MC963G/MC863G

Positive Logic: $4 = \overline{2 \cdot 3}$

Negative Logic: $4 = \overline{2 + 3}$

Input Loading Factor = 1

Output Loading Factor:
MC962/MC862 = 8
MC963/MC863 = 7

Total Power Dissipation:
MC962F/MC862F, P = 33 mW typ/pkg
MC962G/MC862G = 30 mW typ/pkg
MC963F/MC863F,P = 50 mW typ/pkg
MC963G/MC863G = 45 mW typ/pkg

Figure 39 - 3 DTL I.C. Schematic

Procedure:

1. Wire the basic DTL NAND from Figure 39 - 1. Set Swtich A UP. Sketch the waveforms below without and with loads:

DTL NAND WAVEFORMS

Switch B UP Switch C UP	NO LOAD High Level = _____ volts Low Level = _____ volts
Switch B DOWN Switch C UP	RESISTOR LOAD High Level = _____ volts Low Level = _____ volts
Switch B UP Switch C DOWN	CAPACITOR LOAD Rise Time = _____ Fall Time = _____

Although the loading affects amplitude and rise-time, these variations are acceptable in many cases and the DTL INTEGRATED CIRCUITS are useful as DIGITAL LOGIC ELEMENTS.

2. Remove all leads and wire the DTL circuit in Figure 39 - 2. The effects of loading will be the same because the "output-circuit" is the same.

Three Input switches are labeled as (A) , (B) and (C) . The output is denoted as (X) . Each input switch is set UP or DOWN which corresponds to the shorthand digital notation of 1 and 0 (i. e., ONE and ZERO). A positive voltage output is 1 and a ground output is 0.

There are 8 different combinations of the 3 Input Switches. The results of a test of this NAND gate is recorded in a TRUTH TABLE as shown below.

Set the 3 Input Switches at the binary conditions given in the table and record the outputs in the (X) column:

TRUTH TABLE

INPUTS

1 = Switch UP
0 = Switch DOWN

OUTPUT

1 = High volts
0 = Low volts

A	B	C	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

3. A typical Integrated Circuit (I.C.) Dual In-Line Package (D.I.P.) DTL NAND circuit is the I.C. Model No. 862. The PIN Connections are indicated in the diagram below:

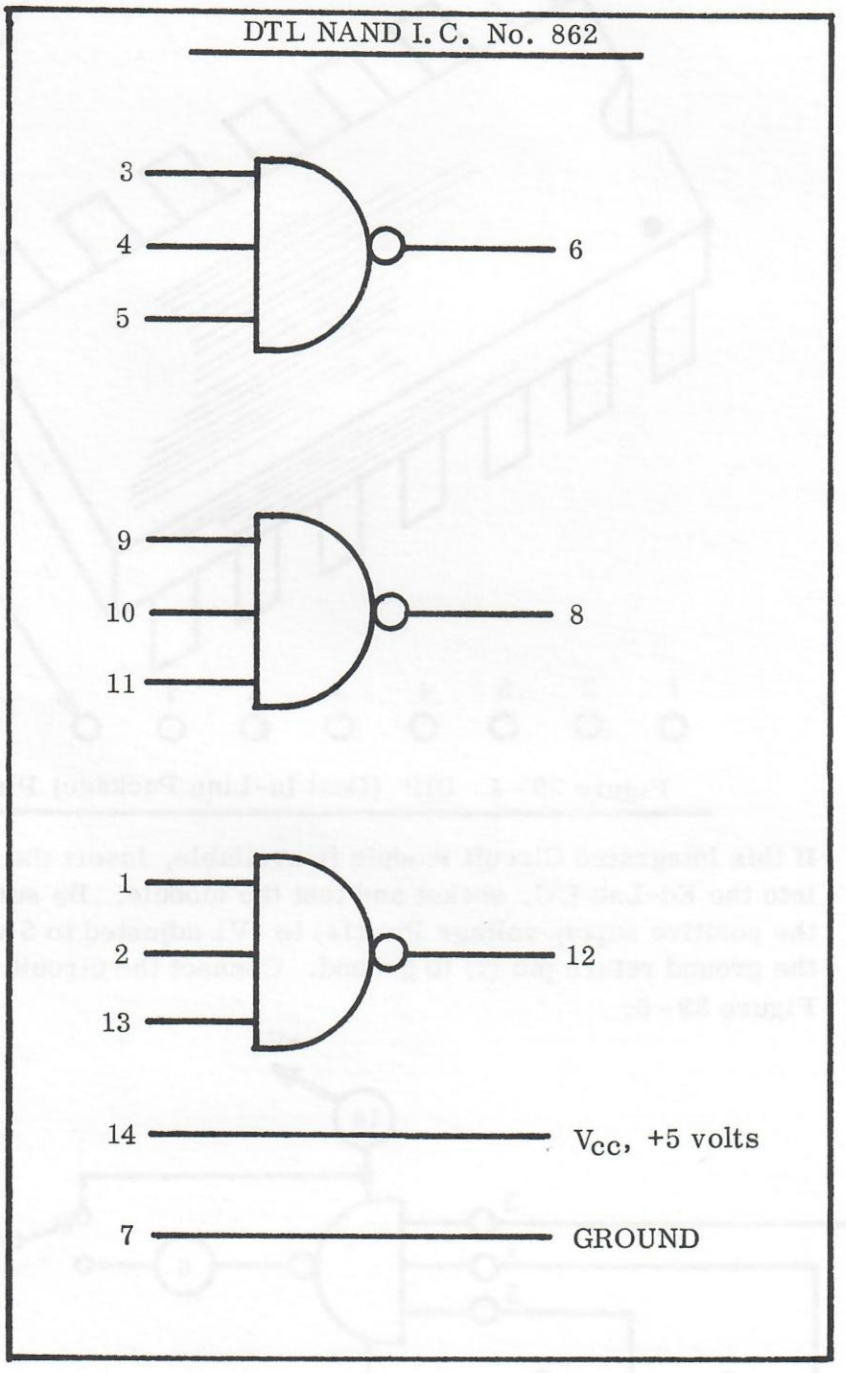


Figure 39-3 NAND Pin Assignment

The DIP Pin Layout is shown below:

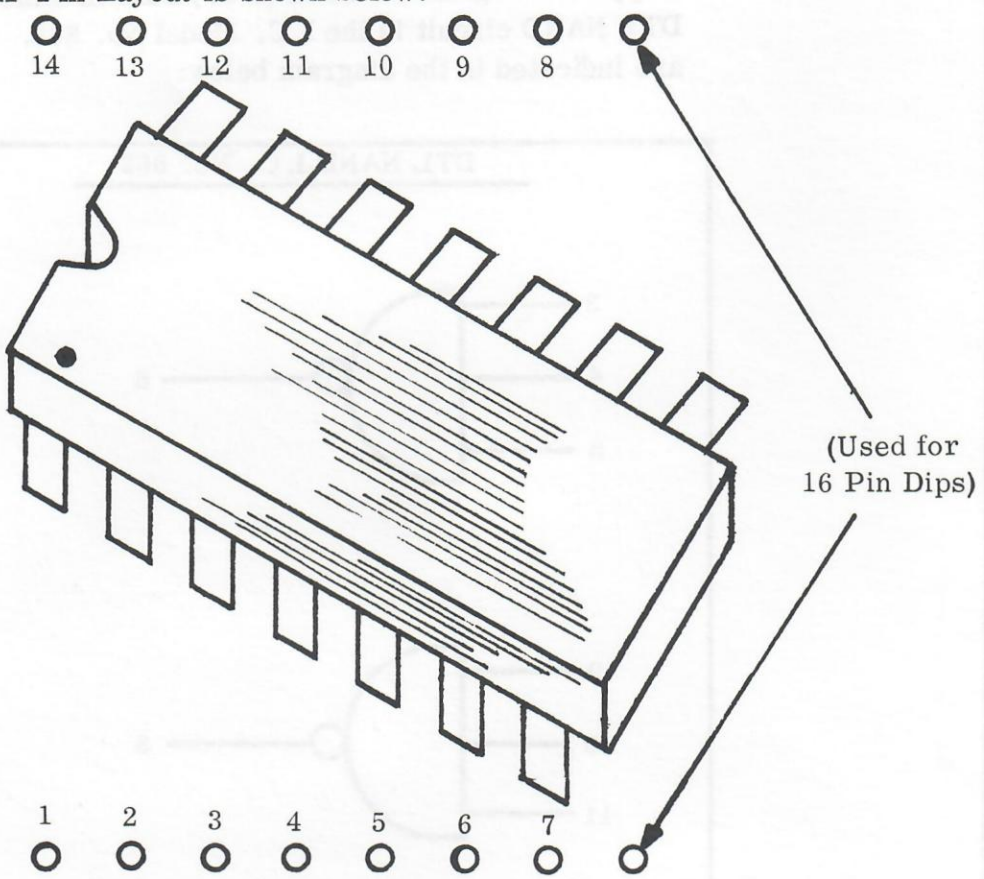


Figure 39-4 DIP (Dual In-Line Package) Pin Layout

4. If this Integrated Circuit module is available, insert the module into the Ed-Lab I.C. socket and test the module. Be sure to connect the positive supply voltage Pin (14) to +V1 adjusted to 5 volts and the ground return pin (7) to ground. Connect the circuit shown in Figure 39-5.

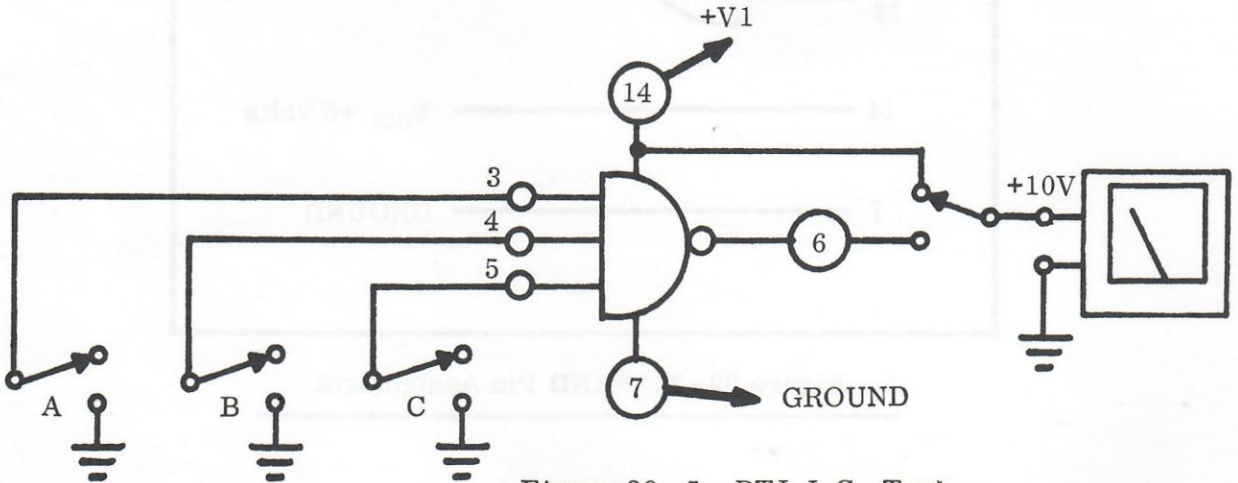


Figure 39-5 DTL I.C. Test

5. Set the input switches in the various conditions shown on the Truth Table and check the output. Does the DTL I.C. operation correspond to the NAND Truth Table?

Ed-Lab	EMITTER FOLLOWER DRIVER	EXP. NO. 40 Page No. 1

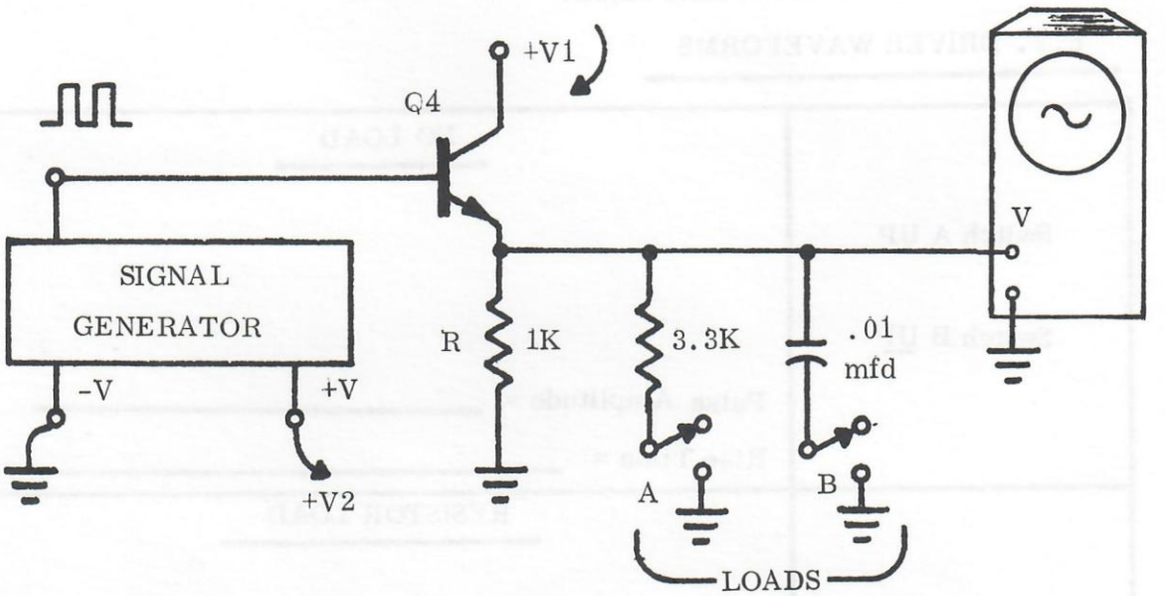


Figure 40 - 1 Emitter Follower Pulse Driver

Objective:

You will use an Emitter Follower or "common collector amplifier" as a pulse driver to reduce the effects of circuit loading.

Description:

The standard Transistor Switch or Inverter circuit is a "common emitter amplifier" and is used as the output driver stage for DTL Logic. Normal load resistance and stray capacitance loads are small and this circuit is acceptable for logic functions. When very high speeds are required for high frequency pulses with corresponding short rise-times, another type of driver must be used. The emitter-follower is the most popular pulse driver circuit. The output is taken from the emitter and the amplifier has a gain of 1. The circuit drives resistor loads very well and provides short rise-times for capacitor loads. But, at high capacitive loads, the transistor is "cut-off" for negative "fall-times" and the fall-time may be large. Most of the time, however, the emitter follower transistor circuit, or the cathode follower vacuum tube circuit, or the source follower FET Field Effect Transistor circuit, are completely acceptable and are used.

Procedure:

1. Wire the circuit in Figure 40 - 1.
2. Test the E.F. Driver circuit without and with the loads.

Ed-Lab	EMITTER FOLLOWER DRIVER	EXP. NO. 40 Page No. 2

Sketch the results below:

E. F. DRIVER WAVEFORMS

Switch A UP Switch B UP	NO LOAD Pulse Amplitude = _____ Rise Time = _____
Switch A DOWN Switch B UP	RESISTOR LOAD Pulse Amplitude = _____
Switch A UP Switch B DOWN	CAPACITOR LOAD Rise Time = _____ Fall Time = _____
Switch A UP Switch B DOWN	CAPACITOR LOAD (Substitute 0.001 mfd CAP.) Rise Time = _____ Fall Time = _____

Ed-Lab	COMPLEMENTARY EMITTER FOLLOWER	EXP. NO. 41 Page No. 1

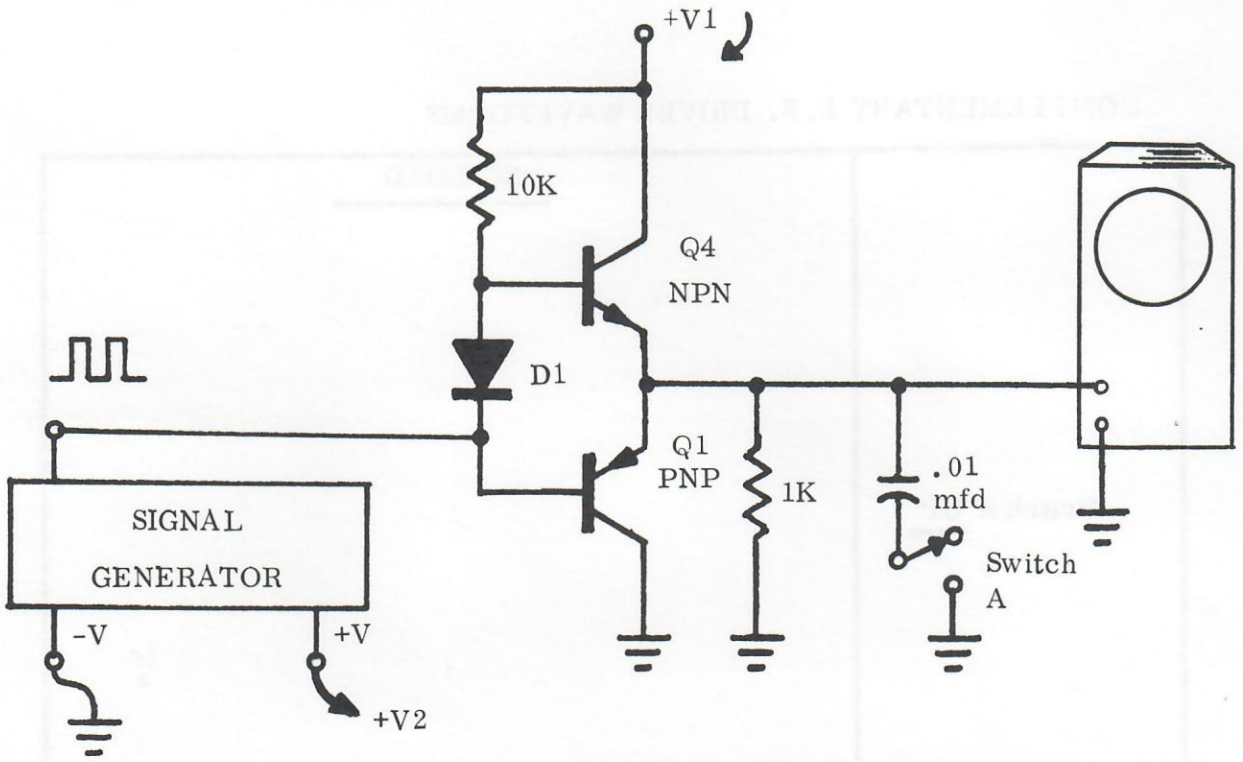


Figure 41 - 1 Complementary Emitter Follower

Objective:

You will use an NPN Emitter Follower and a PNP Emitter Follower to provide a COMPLEMENTARY EMITTER FOLLOWER Driver capable of driving capacitive loads with a sharp rise-time and a sharp fall-time.

Description:

The NPN transistor, Q4, is the Emitter Follower from the previous experiment. The PNP Transistor, Q1, is biased ON when the input decreases and the capacitor discharges through this PNP transistor. The rise and fall times are both thus sharp. The Diode D1 provides a small voltage drop to assure that one of the transistors is always ON. Without this diode, a zero voltage would not hold either transistor ON.

Procedure:

1. Wire the circuit in Figure 41 - 1.
2. Observe the output, with and without the load, and sketch the waveforms on the following page:

COMPLEMENTARY E. F. DRIVER WAVEFORMS

	NO LOAD
Switch A UP	
	CAPACITOR LOAD
Switch A DOWN	

Ed-Lab	TOTEM POLE DRIVER	EXP. NO. 42 Page No. 1

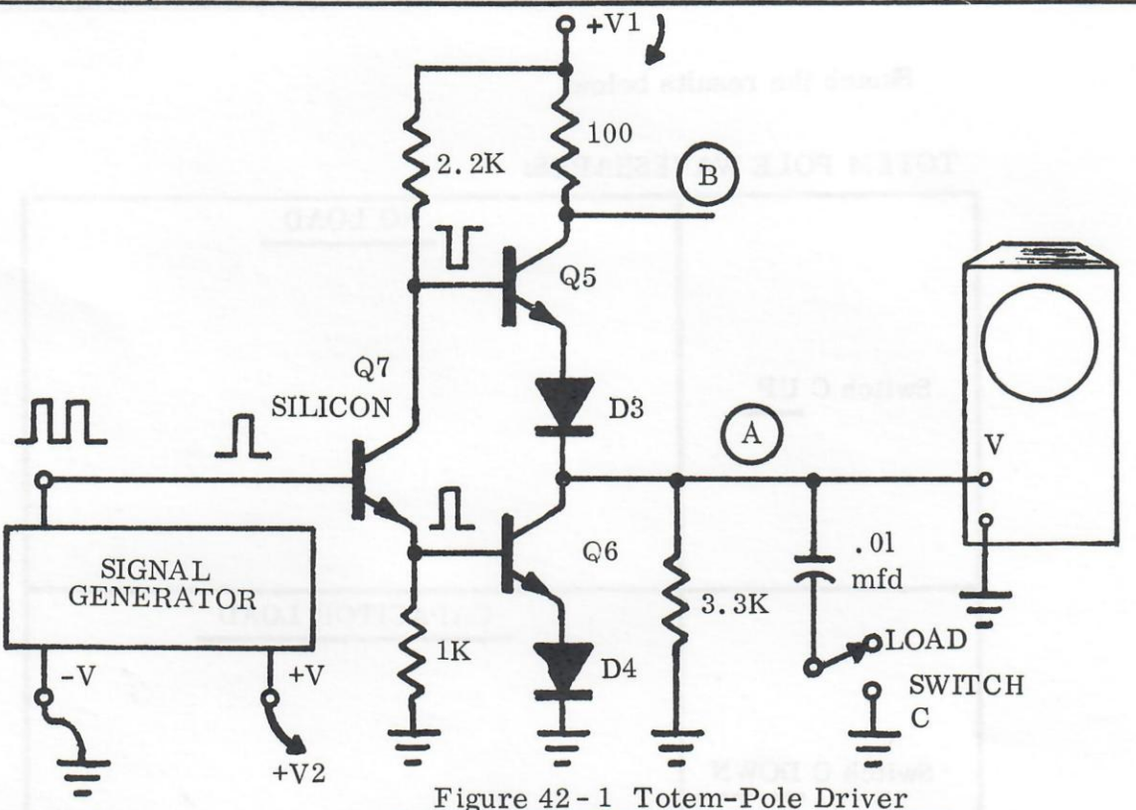


Figure 42 - 1 Totem-Pole Driver

Objective:

You will use two NPN Transistors in a TOTEM POLE PULSE DRIVER Circuit. An NPN Phase Splitter Driver is also used.

Description:

The Transistor Switch or Common-Emitter Amplifier (Q6) provides sharp fall-time to zero volts. The Emitter Follower (Q5) provides sharp rise-times to positive volts. The TOTEM POLE Driver can be considered as a combined emitter follower and transistor amplifier. Because the amplifier transistor (Q5) provides an "inversion" both output transistors must be driven by "inverted-phases". The transistor driver, Q7, provides emitter and collector outputs of opposite "phases" and is called a "phase-splitter". The Diodes provide extra bias thresholds as described in previous experiments.

Procedure:

1. Wire the circuit in Figure 42 - 1.
2. Observe the outputs with and without the capacitive loads.

Sketch the results below:

TOTEM POLE WAVESHAPES:

Switch C UP	NO LOAD
Switch C DOWN	CAPACITOR LOAD

3. A standard common emitter amplifier could have been used with a 100 ohm collector resistor to result in the same short rise-time. The disadvantage of the normal common emitter amplifier is that at a 0 output voltage, full current flows through the 100 ohms to ground. In the totem pole circuit, there is no current flow except through the load resistor. This is demonstrated by observing the voltage across the 100 ohm resistor. This voltage corresponds to the current through the resistor (I = V/R).

   Connect the Oscilloscope to Point B. Keep switch C DOWN with the capacitor load in the circuit. Sketch the waveshape at Point B on the following page:

TOTEM-POLE CURRENT WAVEFORM

POINT (B) : (CURRENT WAVEFORM)

Pulse Voltage Amplitude = _____ volts

4. Calculate and describe the collector current.

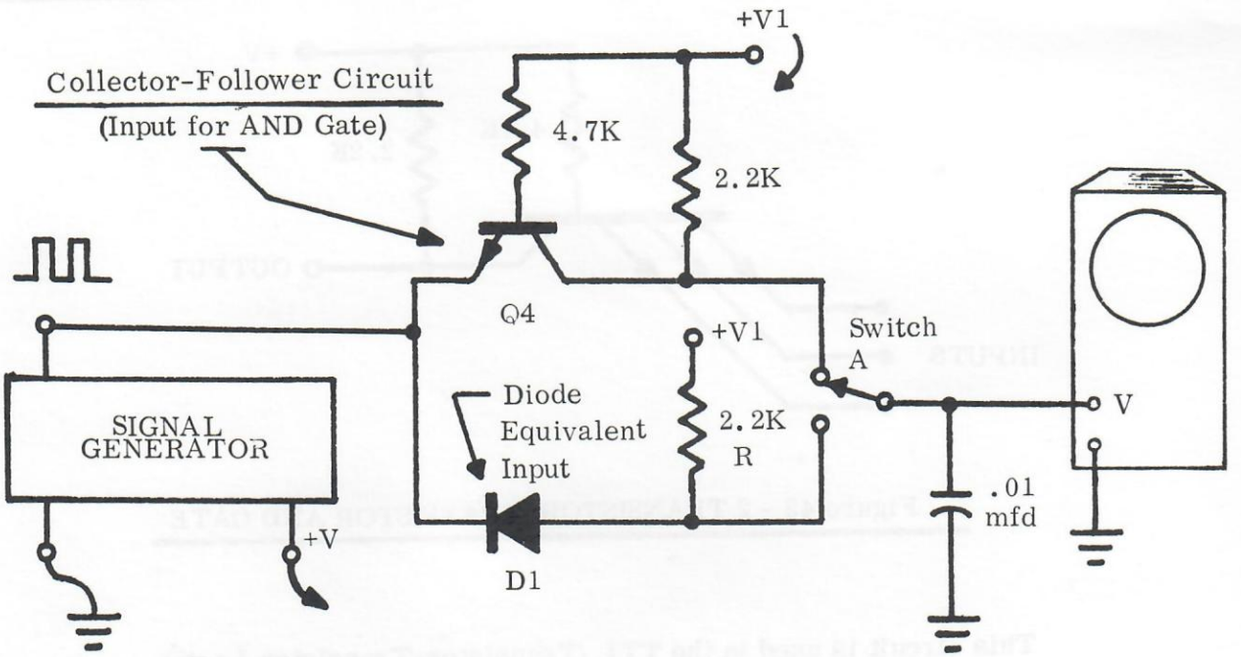


Figure 43 - 1 Collector Follower

Objective:

You will compare the operation of a DIODE AND gate circuit with a TRANSISTOR AND gate circuit and you will test a Transistor COLLECTOR FOLLOWER:

Description:

The Diode AND gate uses many diode inputs (only one Diode, D1, is shown above). A Transistor Amplifier (Q4) with an emitter input and collector output is called a "common base amplifier". With a small base resistor, and high input emitter voltages, the transistor is always ON and the collector voltages equal the emitter voltages. This type of circuit is thus sometimes called a "collector follower".

With the Diode AND Input for a positive rising voltage, the diode "opens" and the external stray capacitance load is charged through the resistor R in the "passive" circuit.

With the Transistor AND Input (collector-follower circuit) the transistor continues to conduct and the circuit is an "active" circuit. The rise-time is improved.

The collector-follower is used in Integrated Circuit AND gates with transistors constructed using multiple emitters as sketched on the following page:

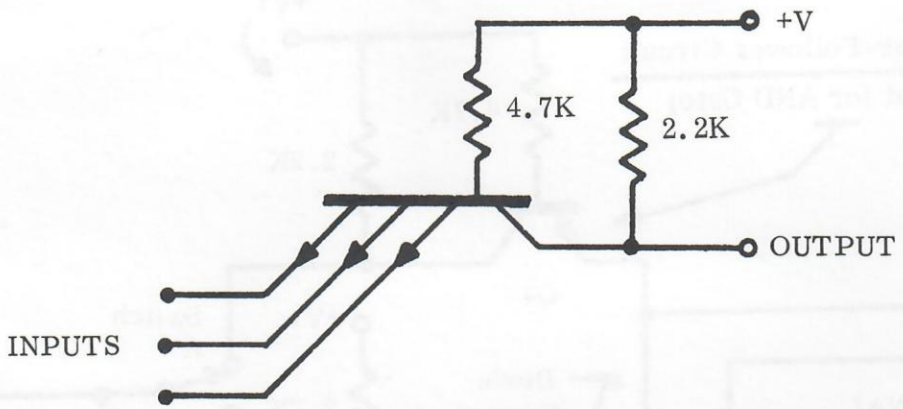


Figure 43 - 2 TRANSISTOR-TRANSISTOR AND GATE

This circuit is used in the TTL (Transistor-Transistor Logic) Integrated Circuits and will be tested in the next experiment.

Procedure:

1. Wire the two complete circuits as shown in Figure 43 - 1. The Switch A selects the DIODE input (Switch A DOWN) or the TRANSISTOR input (Switch A UP). Compare the rise-time and fall-time responses for the two circuits.

"AND" OUTPUT WAVEFORMS:

DIODE INPUT (Switch A DOWN)	TRANSISTOR INPUT (Switch A UP)
Rise Time = _____	Rise Time= _____
Fall Time = _____	Fall Time = _____

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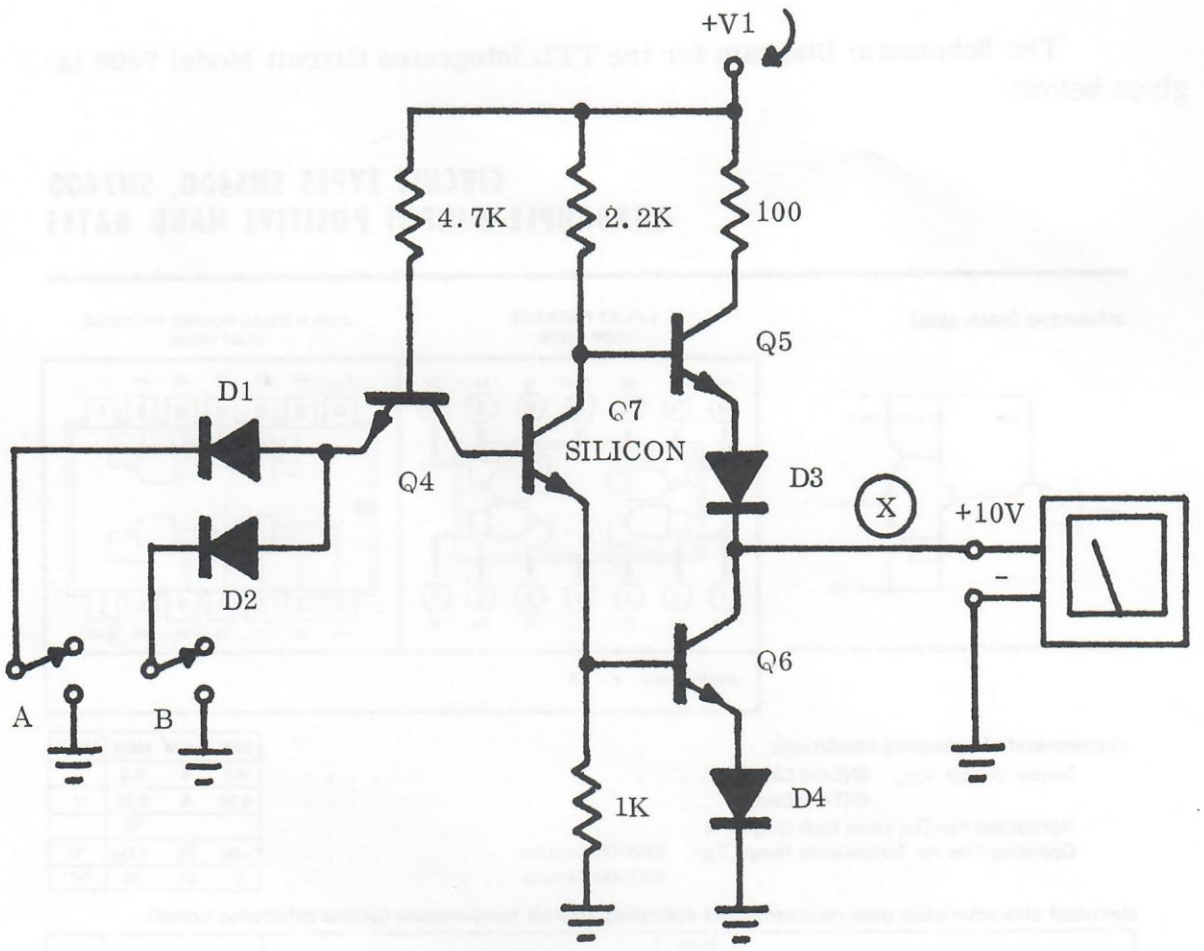


Figure 44 - 1 TTL NAND Circuit

Objective:

You will combine the "Collector Follower AND TTL Circuit" with the Totem Pole Driver to form the TTL NAND Circuit that is used in the 7400 Series Digital Integrated Circuits.

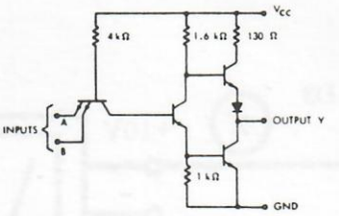
Description:

The Collector Follower AND from the previous experiment is connected to two input DIODES. In the standard TTL Integrated Circuits, the transistor has many emitters which are the AND gate inputs.

The Schematic Diagram for the TTL Integrated Circuit Model 7400 is given below:

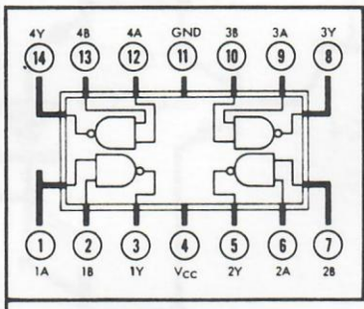
CIRCUIT TYPES SN5400, SN7400
QUADRUPLE 2-INPUT POSITIVE NAND GATES

schematic (each gate)

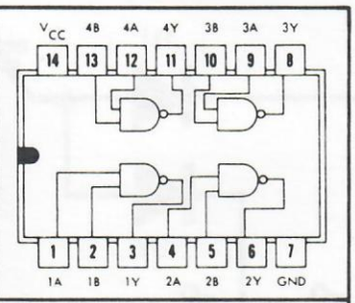


NOTE: Component values shown are nominal.

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5400 Circuits	4.5	5	5.5	V
SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5400 Circuits	−55	25	125	°C
SN7400 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5400	−20		−55	mA
				SN7400	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0			4	8	mA

Figure 44 - 2 TTL I.C. NO. 7400 Schematic

The I.C. Dual-In-Line (DIP) Package pin mechanical layout is the same as for the DTL I.C. with pins specified as 1 through 14.

The Logic Circuit Pin assignment is shown below:

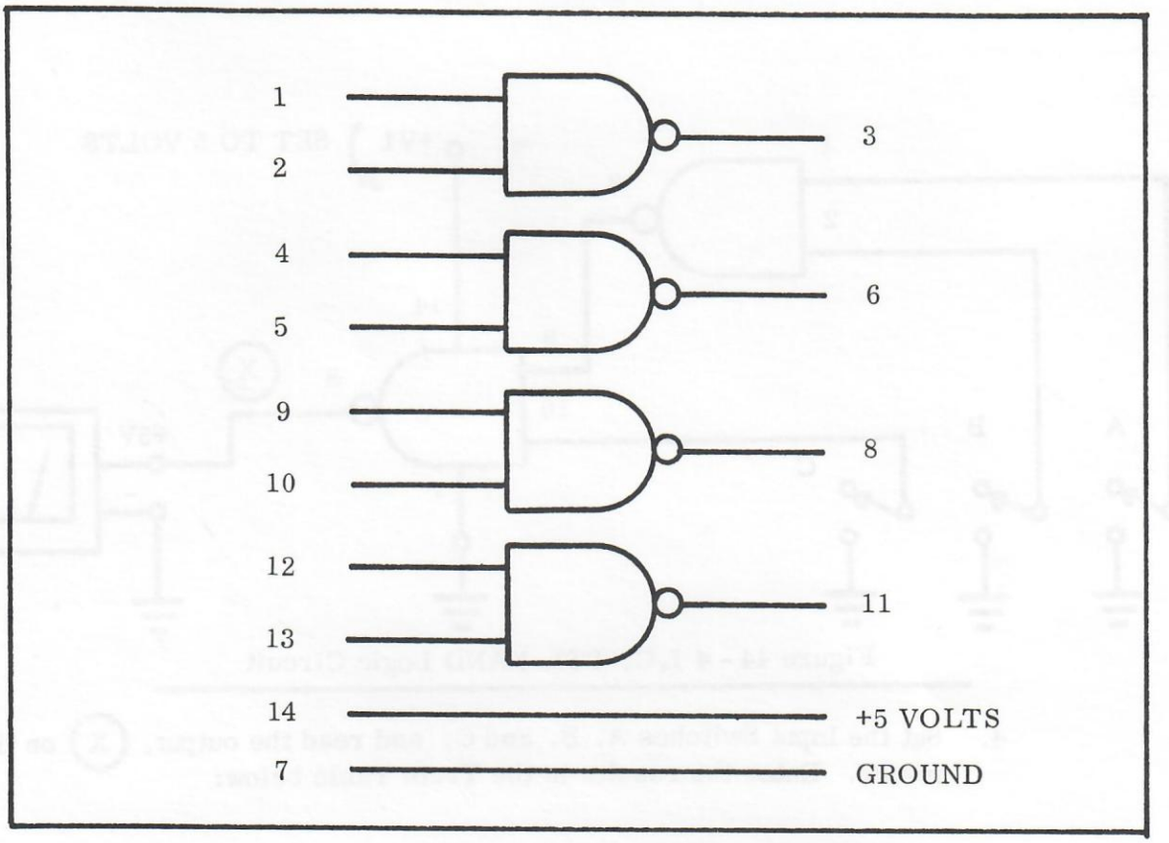


Figure 44 - 3 TTL 7400 Pin Layout

Procedure:

1. Wire the TTL Circuit in Figure 44 - 1.
2. Set the input switches in the 4 different input conditions and record the output in the Truth Table below:

TTL NAND

A	B	X
0	0	
0	1	
1	0	
1	1	

Are the results correct?

3. If a TTL NAND 7400 is available, plug this I.C. Module into the I.C. Socket. Be sure to connect +V1 adjusted to 5 volts and connect ground to the I.C. Wire the circuit in Figure 44 - 4

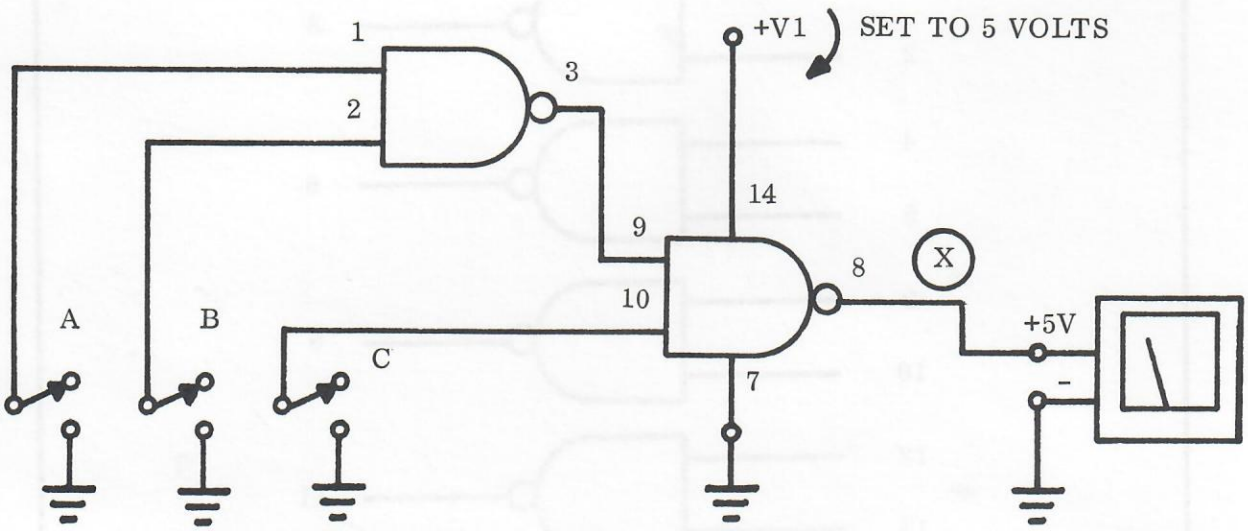


Figure 44 - 4 I.C, TTL-NAND Logic Circuit

4. Set the Input Switches A, B, and C; and read the output, (X) on the meter. Enter the results in the Truth Table below:

INPUT			OUTPUT
A	B	C	X

1 = UP
0 = DOWN (Ground)

1 = ON (Hi volts)
0 = OFF (Lo volts)

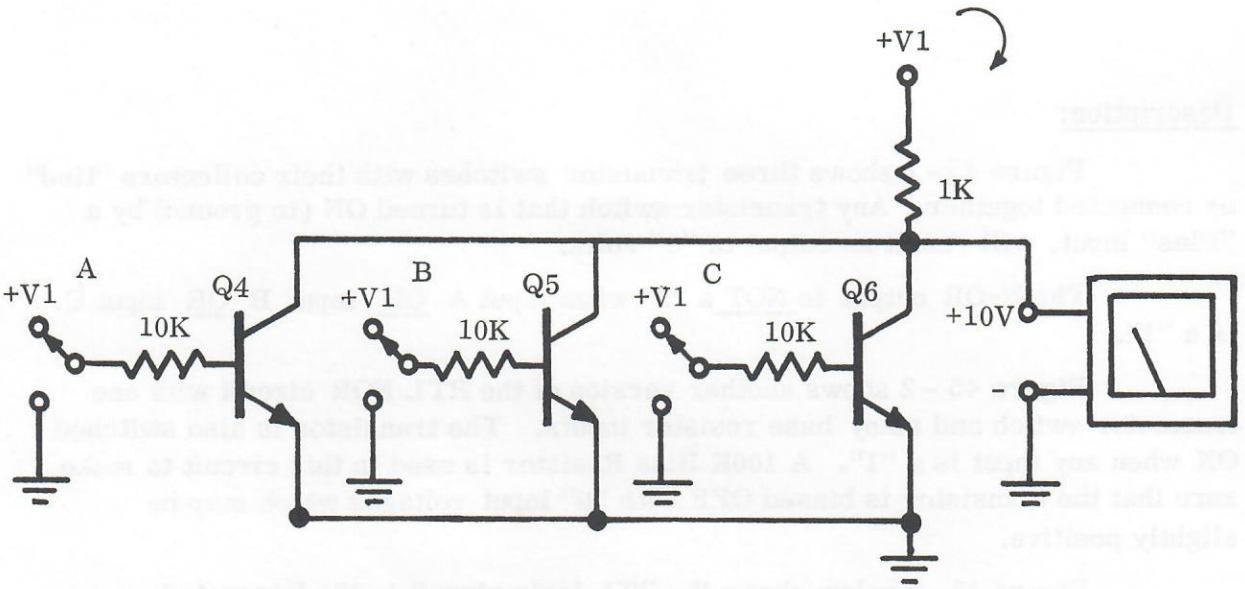


Figure 45 - 1. RTL NOR - Transistor Circuit

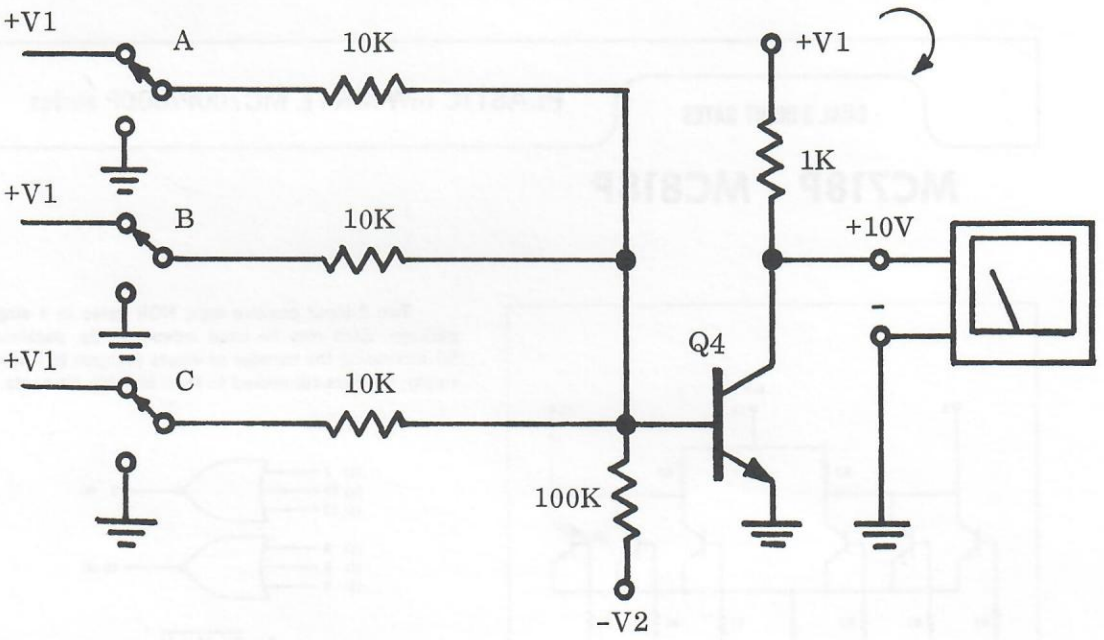


Figure 45 - 2. RTL NOR - Resistor Circuit

Objective:

You will use the TRANSISTOR SWITCH circuit with multiple inputs to perform the NOT - OR Logic Function in an RTL - NOR circuit (Resistor - Transistor - Logic).

Description:

Figure 45-1 shows three transistor switches with their collectors "tied" or connected together. Any transistor switch that is turned ON (to ground) by a "Plus" Input, will result an output of "0" volts.

The N-OR output is NOT a "1" when input A OR input B OR input C is a "1".

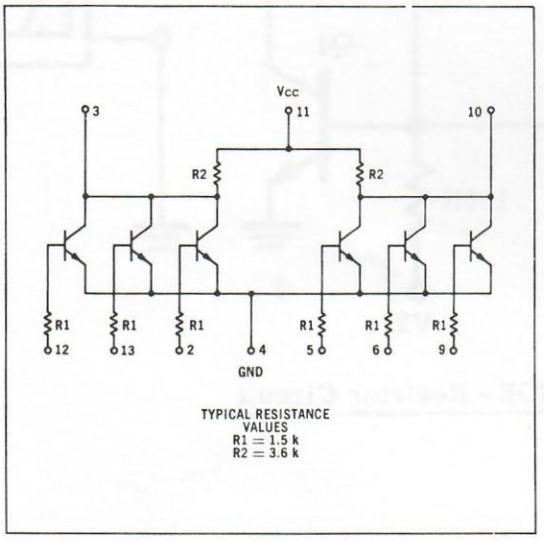
Figure 45 - 2 shows another version of the RTL NOR circuit with one transistor switch and many base resistor inputs. The transistor is also switched ON when any input is a "1". A 100K Bias Resistor is used in this circuit to make sure that the transistor is biased OFF with "0" input voltages which may be slightly positive.

Figure 45-3 below shows the RTL logic circuit in the Integrated Circuit Model No. 718.

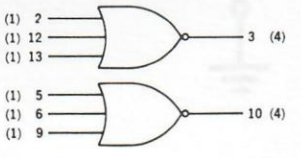
DUAL 3-INPUT GATES

PLASTIC mW MRTL MC700P/800P series

MC718P • MC818P



Two 3-input positive logic NOR gates in a single package. Each may be used independently, paralleled for increasing the number of inputs (subject to loading rules), or cross-connected to form bistable elements.



$3 = \overline{2 + 12 + 13}$

NUMBER IN PARENTHESIS INDICATES MC718P, MC818P LOADING FACTOR

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5mW (Inputs Low)

Figure 45-3 RTL I.C. 718

Procedure:

1. Wire the circuit in Figure 45 - 1.
2. Set the input switches and record the output in the Truth Table below:

A	B	C	NOR Fig. 45-1	NOR Fig. 45-2	NAND Fig. 45-3
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

3. Wire the NOR circuit in Figure 45 - 2.
4. Set the input switches and record the output in the proper columns above.

   Do both circuit outputs correspond to the NOR ?
5. When the Transistor switches are connected in a "Totem-Pole" or in "Cascade" or in "Series", the resulting circuit is shown on the following page:

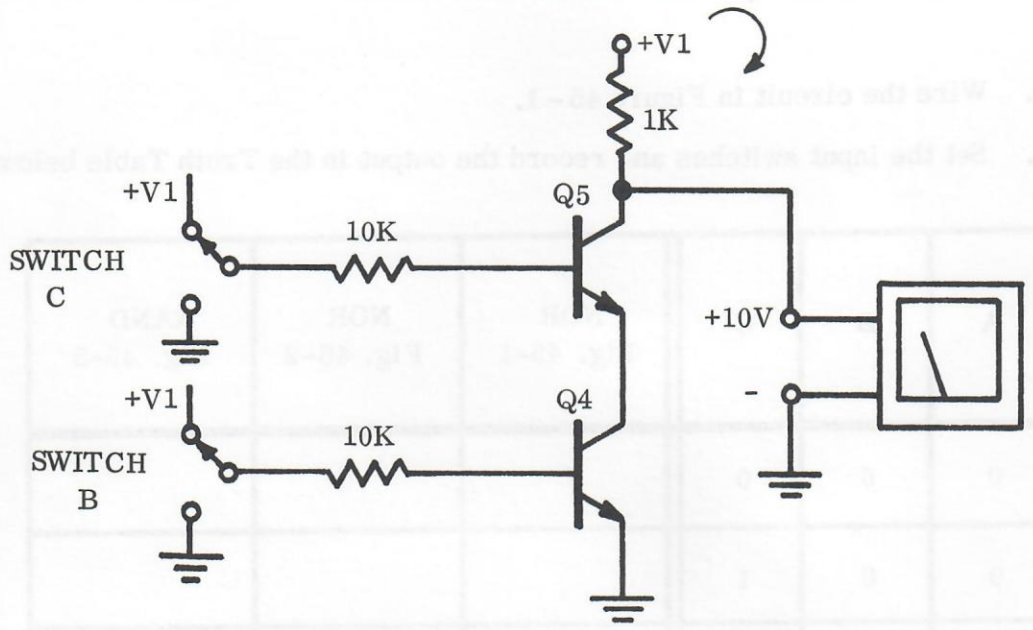


Figure 45-3 Transistor NAND

The output will be a "0" or ground only when both swtiches are ON.

The output is NOT a "1" when input A AND input B are "1". The circuit is then a NOT - AND or a NAND.

6. Wire the circuit in Figure 45 - 3.
7. Operate the input switches and enter the results in the last column in the Truth Table.
8. Do the results correspond to the NAND function?
9. The RTL - NOR Integrated Circuit No. 718 is a DUAL 3 - INPUT NOR. The Pin Layout is shown below:

V_{cc} 11
GND 4

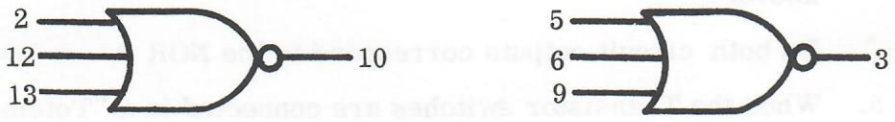


Figure 45-4. No. 718 NOR Pin Layout

10. If the No. 718 I.C. is available, wire the NOR logic system shown below in Figure 45-5.

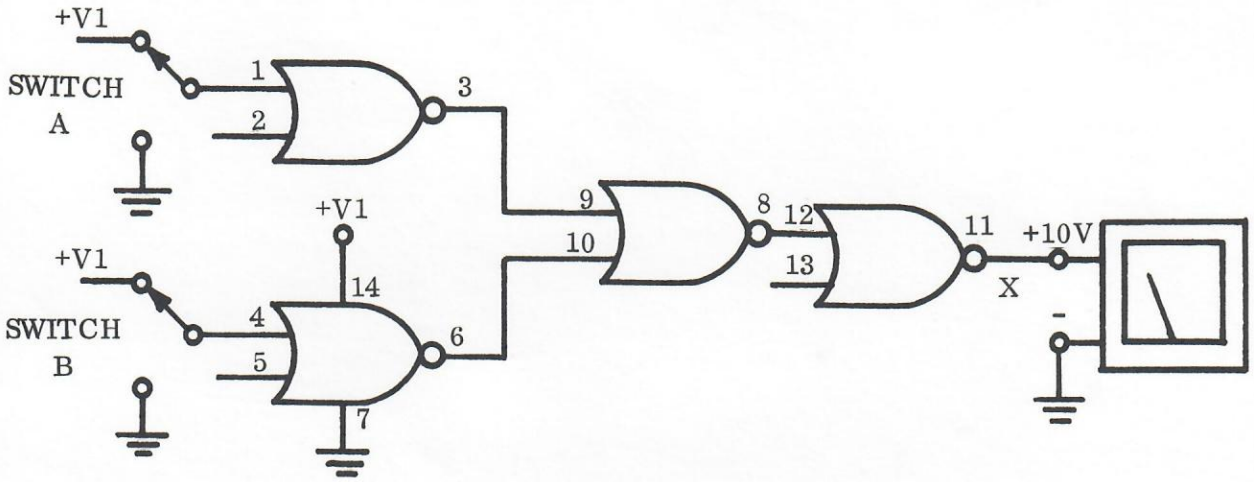


Figure 45-5. NOR Logic System

11. Test the NOR Logic System and enter the results in the Truth Table below:

INPUTS		OUTPUT
A	B	X
0	0	
0	1	
1	0	
1	1	

12. By reviewing the Truth Table, what logic "function" does this NOR Logic System perform?

A	B	X
0	0	
0	1	
1	0	
1	1	

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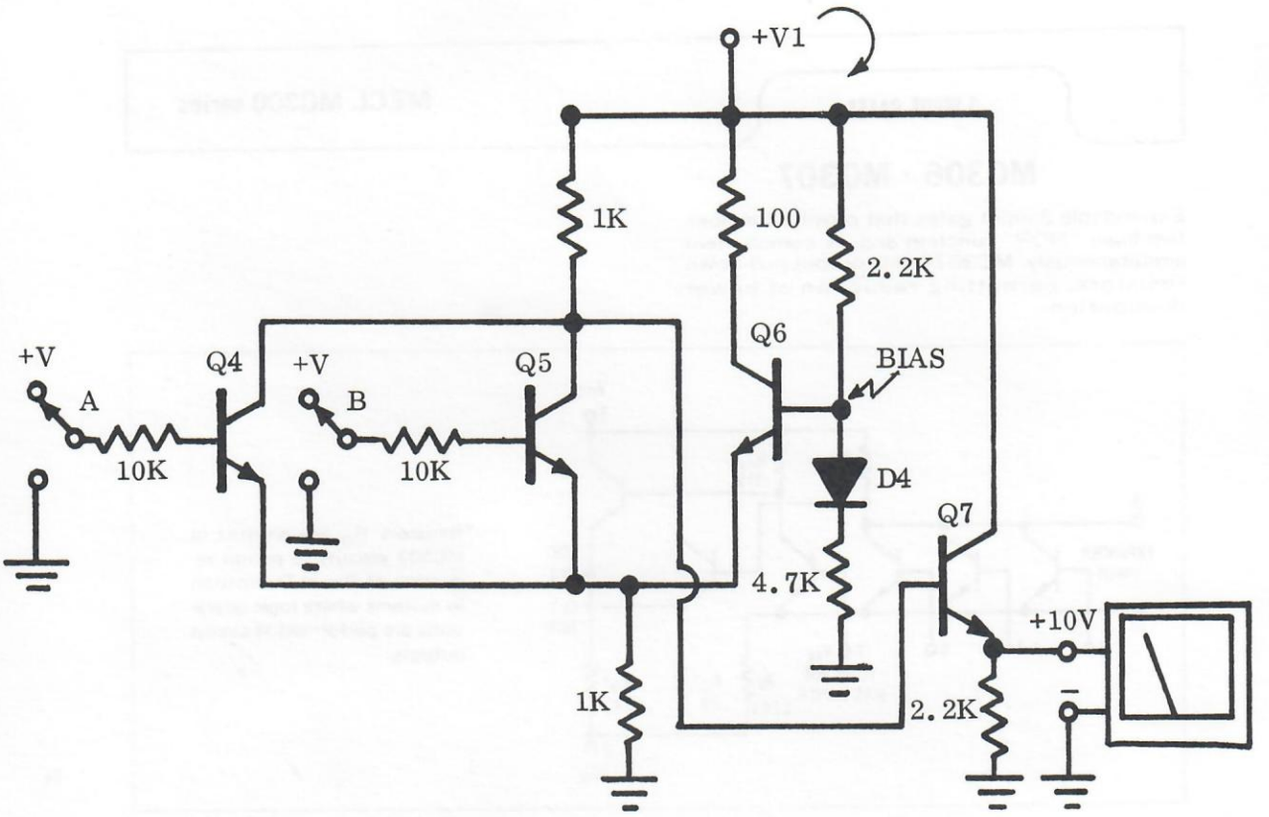

Figure 46-1 Emitter Coupled Logic NOR Circuit

Objective:

You will test the operation of the Emitter Coupled Logic or ECL NOR circuit.

Description:

The Emitter Coupled circuit shown in Figure 46 - 1 resembles the "Difference Amplifier" circuit with the emitter-coupling. The BIAS Level is preset. Low inputs at A and B will keep transistors Q4 and Q5 biased OFF and their collector voltage will be at +V. The output is taken from the collector through the emitter follower using transistor, Q7. When input A OR input B are at +VOLTS (i.e., "1"), transistors Q4 or Q5 are ON and the collector voltage drops to a level determined by the collector and emitter resistors, and by the BIAS voltage. This circuit resembles the RTL NOR except for the emitter resistor, the bias transistor (Q6), and the emitter follower output. The advantage of this circuit is that the transistors are biased to be always ON, at either high or low voltages (i.e., 1 or 0) and the result is a very high speed of operation. The ECL Circuit for I.C. Model No. 306 is shown on the following page:

3-INPUT GATES

MECL MC300 series

MC306 · MC307

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC307 omits output pull-down resistors, permitting reduction of power dissipation.

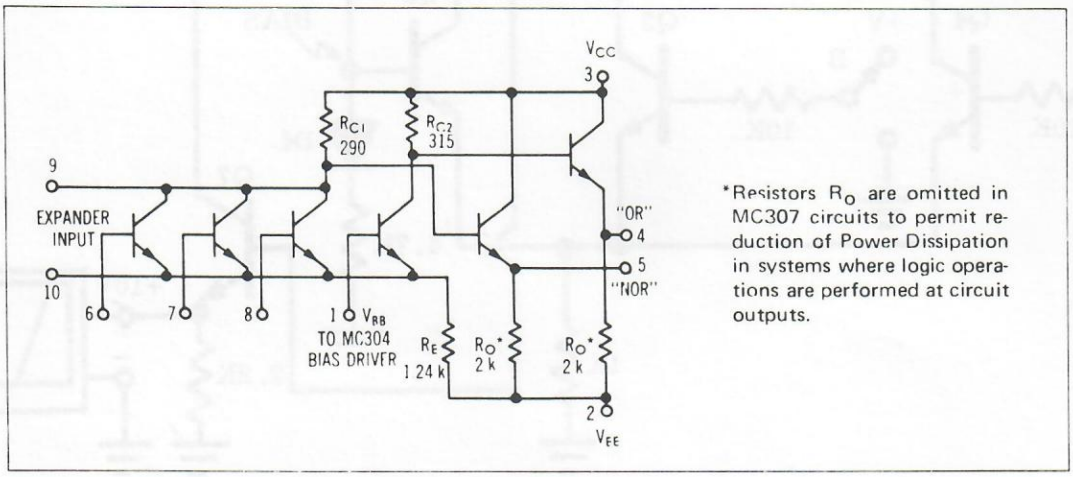

Figure 46-2 I.C. No. 306 ECL NOR

Procedure:

1. Wire the circuit in Figure 46-1.
2. Operate the input switches and record the outputs in the Truth Table.

   Measure the output voltage levels for a LOW or 0, and for a HIGH or 1 and enter the results in the table below:

Binary Output	Voltage
High (1)	
Low(0)	

Enter the Truth Table results below:

ECL NOR

INPUTS		OUTPUT
A	B	X
0	1	
1	0	
1	1	
0	0	

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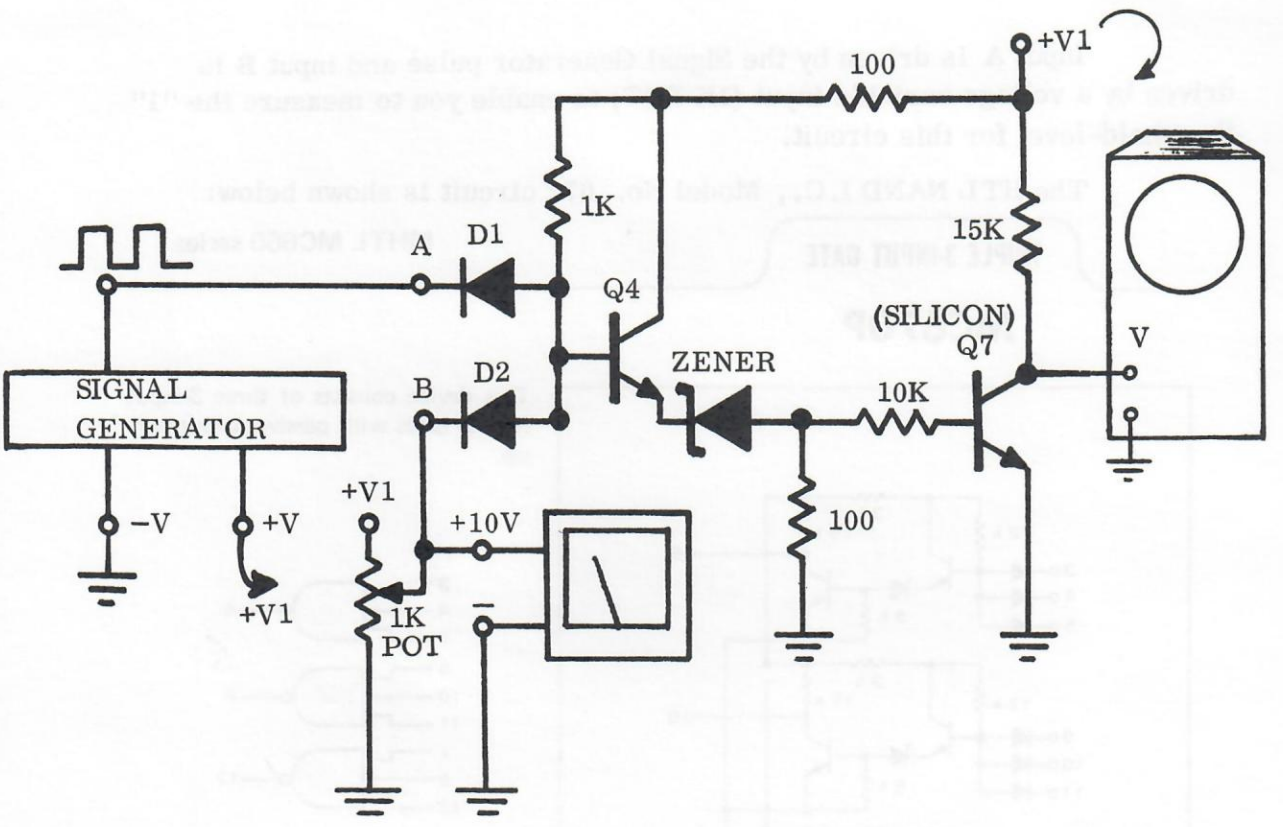


Figure 47-1 HTL NAND Circuit

Objective:

You will test the operation of the HIGH THRESHOLD LOGIC/HTL-NAND circuit.

Description:

The NAND circuit in Figure 47-1 is basically a DIODE "AND" gate, followed by an EMITTER FOLLOWER (Q4), followed by a Transistor (switch) INVERTER or NOT (Q7). The Zener diode acts as a series "battery" and provides "threshold". The input must rise above this threshold voltage level before the output transistor is turned ON. The High Threshold Logic circuits are used in Industrial factories where there are many motors and relays causing electrical noise voltages.

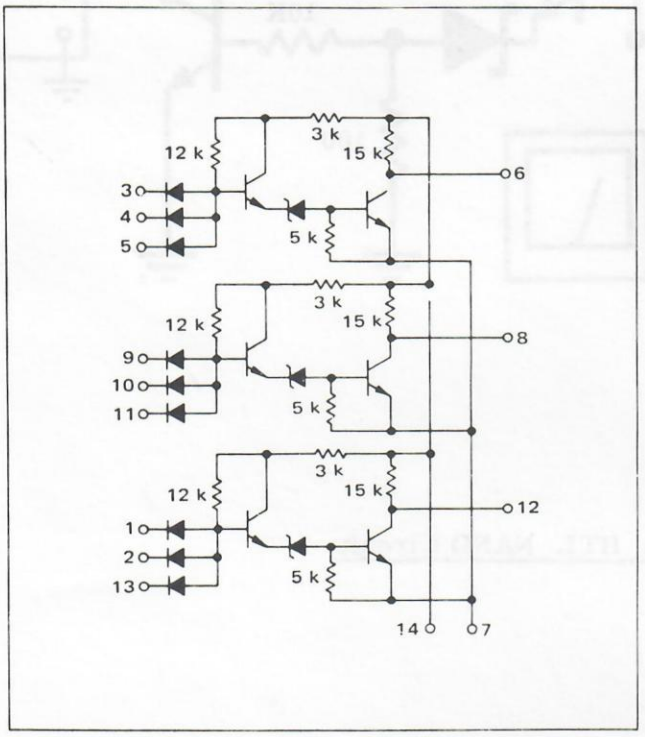
Input A is driven by the Signal Generator pulse and input B is driven by a voltage variable input (1K POT) to enable you to measure the "1" threshold-level for this circuit.

The HTL NAND I.C., Model No. 670 circuit is shown below:

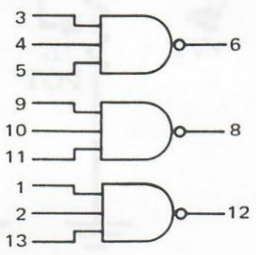
TRIPLE 3-INPUT GATE

MHTL MC660 series

MC670P



This device consists of three 3-input NAND gates with passive output pull-up.



Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Input High = 132 mW
Inputs Low = 39 mW

Figure 47-2 I.C. No. 670 HTL NAND

Procedure:

1. Wire the circuit in Figure 47 - 1.

   Observe the output on the oscilloscope.

2. Adjust the 1K POT for the Input B voltage level.

   When the input is "0", there are not output pulses.

   When the input is "1" the input A pulses appear at the output (inverted).

3. Vary the 1K POT and determine the "0" and "1" input voltage levels. Enter the results on the following page:

INPUT B	VOLTAGE
"0"	0 to _____ volts
"1"	_____ volts to _____ volts

Digital Integrated Circuits

Monolithic Silicon

CD4000A Series

COS/MOS IC's for Low-Voltage (3-15V) Applications

COS/MOS features:

- Low power — 10 nW typ. for gates 10 μW typ. for MSI circuits
- Wide voltage range 3 to 15 volts (1.3 volts for special types)
- High noise immunity — 45% of supply voltage (typ.)
- High speed — to 10 MHz for gates and flip flops to 5 MHz for counters and registers
- Logic compatibility T^2L & DTL interfacing (see ICAN 6602)
- High fanout

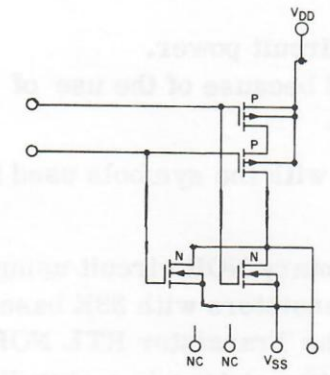


Figure 48-1 C-MOS I.C. CIRCUIT

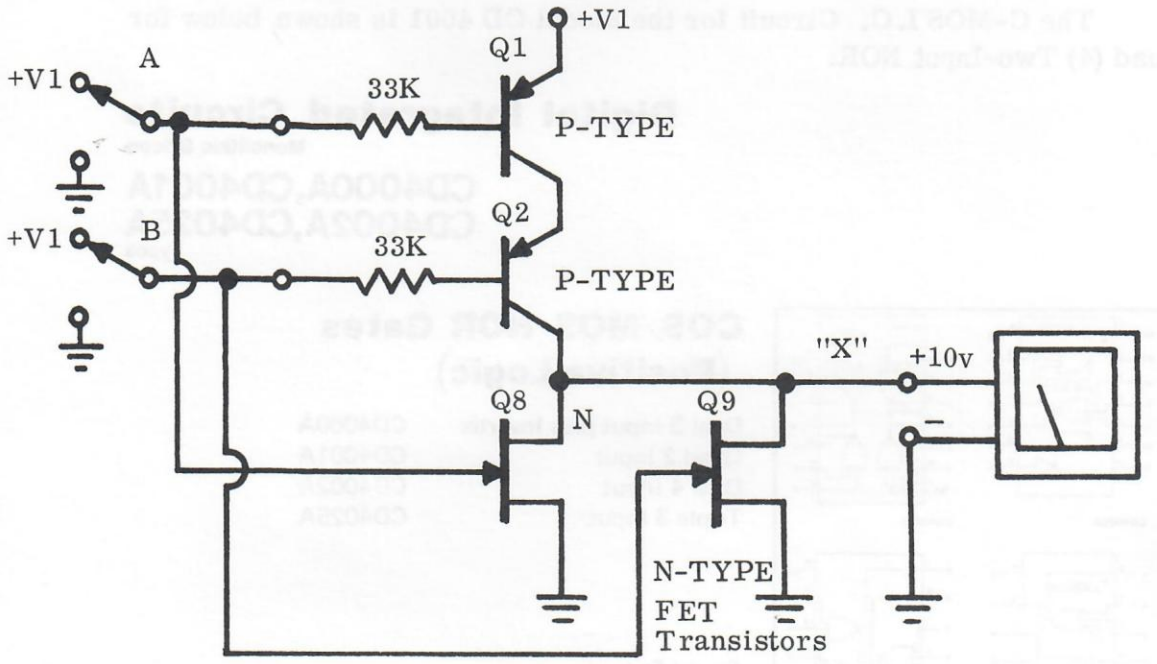


Figure 48-2 C-MOS NOR Circuit Experiment

Objective:

You will connect N-Type and P-Type semiconductors in a Complementary NOR circuit similar to that used in C-MOS Integrated Circuits.

Description:

The letters MOS are abbreviations for "Metal Oxide Silicon" which refers to a method for constructing semiconductors. The advantages of this method are:
1: Very small circuit construction can be achieved resulting in many "thousands" of circuits in a single small Integrated Circuit , and
2: Use of a "Field-Effect" which results in very low circuit power.
The letter C in C-MOS is for "Complementary" - MOS because of the use of "complementary" P-Type and N-Type Semiconductors.

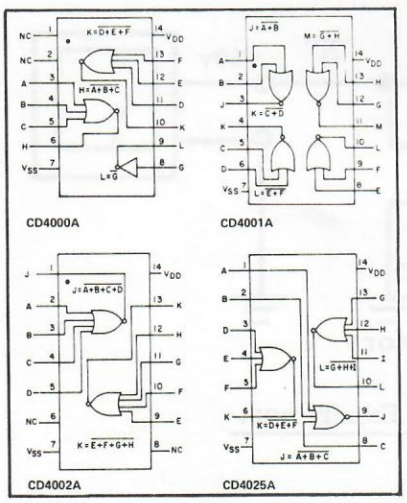
Figure 48 - 1 shows the C-MOS NOR circuit with the symbols used for the I.C. MOS construction.

Figure 48-2 shows the equivalent complementary NOR circuit using two FET N-Type Semiconductors, and two P-Type Transistors with 33K base resistors. The N-Type Semiconductors are arranged similar to the Transistor RTL NOR circuit. The equivalent collector resistor is replaced with two transistors in a circuit similar to the "common-emitter amplifier" which is connected with a "reverse polarity" because of the P-Type material.

The C-MOS I.C. Circuit for the model CD 4001 is shown below for the Quad (4) Two-Input NOR:

Digital Integrated Circuits
Monolithic Silicon

CD4000A, CD4001A
CD4002A, CD4025A
Types



COS/MOS NOR Gates
(Positive Logic)

Dual 3 Input plus Inverter	CD4000A
Quad 2 Input	CD4001A
Dual 4 Input	CD4002A
Triple 3 Input	CD4025A

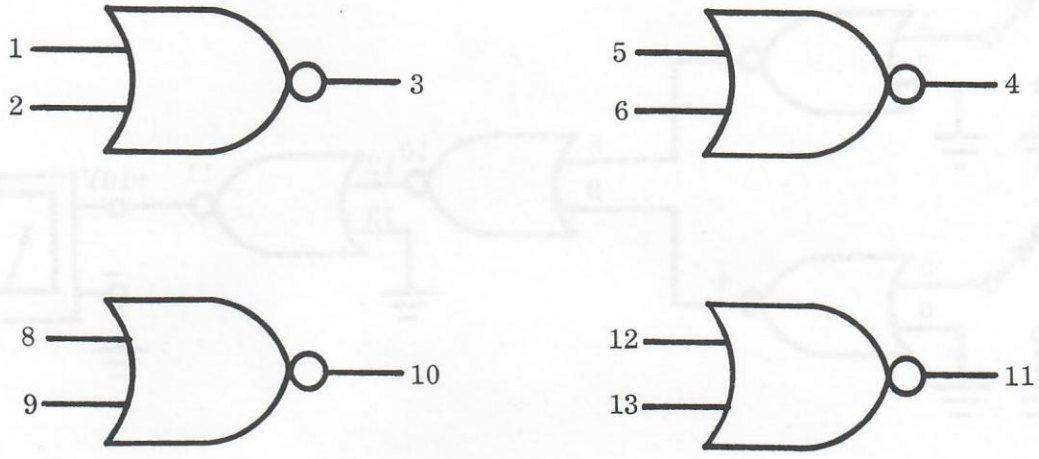
Special Features

- Medium speed operation..... $t_{PHL} = t_{PLH} = 25$ ns (typ.) at $C_L = 15$ pF
- Low "high"- and "low"-level output impedance..... 500Ω and 200Ω (typ), respectively at $V_{DD} - V_{SS} = 10$ V

The combination of these devices and the RCA NAND positive logic gate types CD4011A, CD4012A, and CD4023A can account for appreciable package-count savings in various logic function configurations.

Figure 48-3 C-MOS I.C. No. CD 4001

The pin assignments are illustrated below:



V_{DD} ——— PIN 14

V_{SS} ——— PIN 7

Figure 48-4 C-MOS 4001 A

Procedure:

1. Wire the experiment circuit in Figure 48-2.
2. Set the Switch Inputs at the 4 different input conditions. Enter the results below:

INPUT		OUTPUT
A	B	X
0	0	
0	1	
1	0	
1	1	

Do the results correspond to the NOR logic?

3. If an I.C. Model CD 4001 is available, insert this I.C. in the socket and test the NOR operation. Wire the logic in Figure 48-5 below:

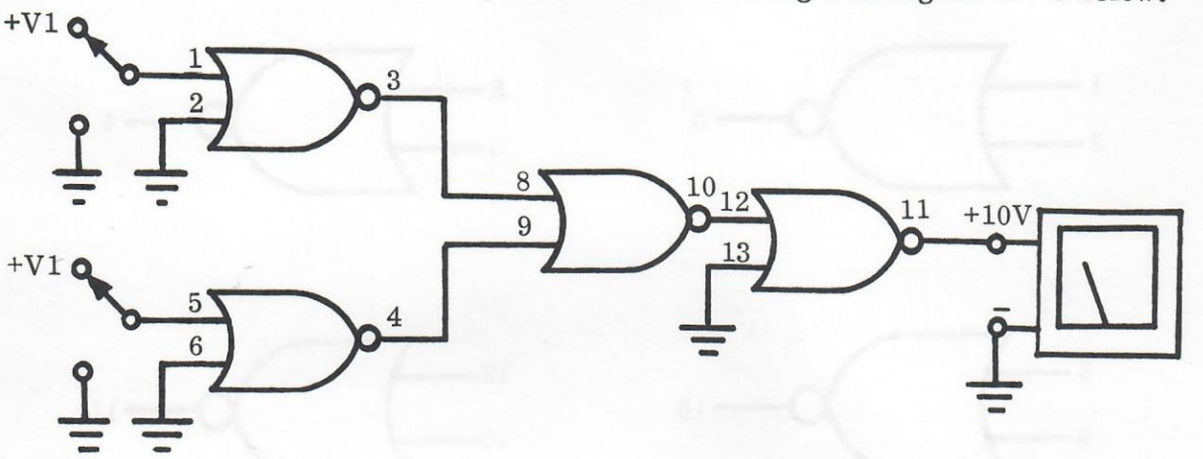


Figure 48-5 C-MOS Logic System

Enter the results in the Table below:

INPUTS		OUTPUT
A	B	X
0	0	
0	1	
1	0	
1	1	

What logic function does the above logic system perform?

Ed-Lab | CAPACITIVE COMPENSATION ATTENUATOR | EXP. NO. 49 Page No. 1

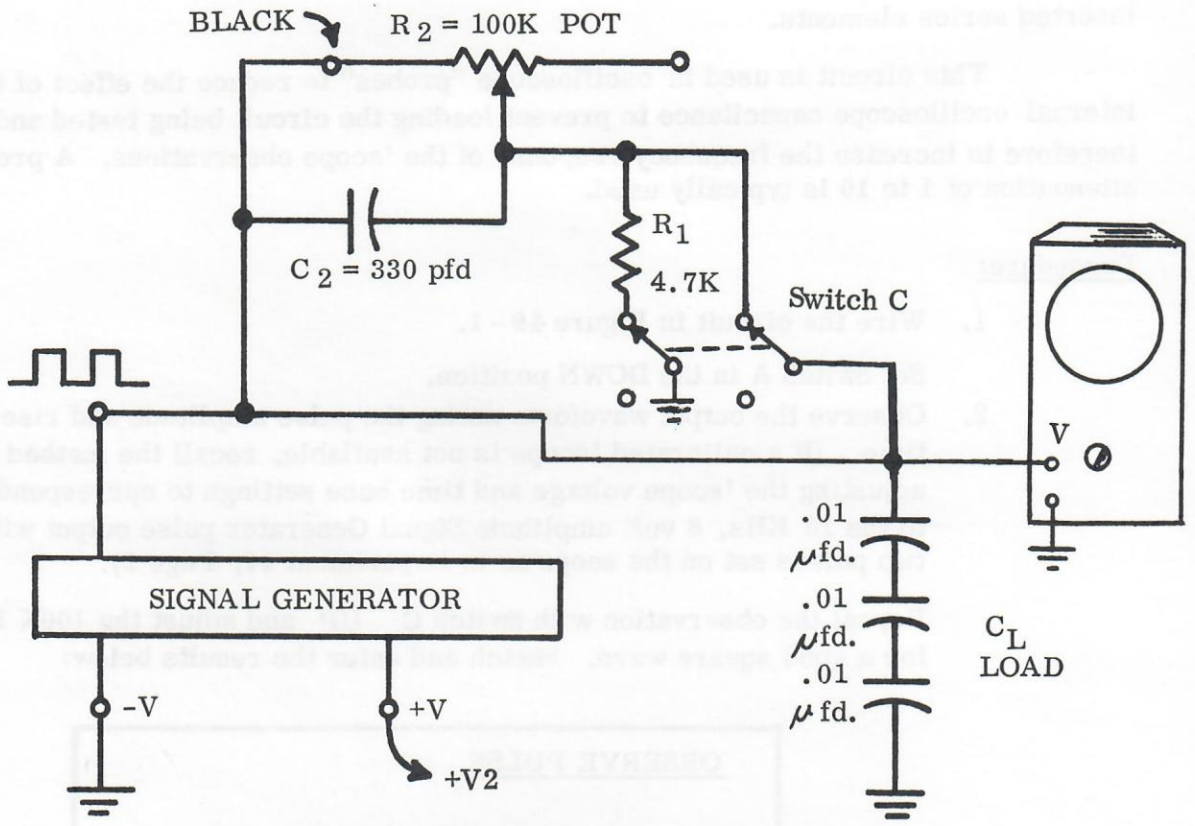


Figure 49-1 Capacitive Compensation Attenuator

Objective:

You will use a Series R - C ATTENTUATION CIRCUIT to greatly reduce the effects of Capacitive Loading.

Description:

The Signal Generator output stage is a common emitter amplifier with a collector resistor, R_c, of 2.2K. With Switch A, DOWN, the Capacitive LOAD applied to the Signal Generator output is 3 series 0.01 μfd capacitors (C_L = 3,300 pfd) This results in a long rise-time for the output pulse given by the time constant, $R_c C_L$.

The method used to improve the rise time is to insert a series resistor and capacitor, R_2 and C_2, and a parallel load resistor R_1. When the series time constant, $R_2 C_2$, equals the load time constant, $R_1 C_L$, there is perfect frequency response at all frequencies and thus also for the square wave pulse. This circuit does however provide an "attenuation" or loss of signal level due to the

inserted series elements.

This circuit is used in oscilloscope "probes" to reduce the effect of the internal oscilloscope capacitance to prevent loading the circuit being tested and therefore to increase the frequency response of the 'scope observations. A probe attenuation of 1 to 10 is typically used.

Procedure:

1. Wire the circuit in Figure 49-1.

   Set Switch A in the DOWN position.

2. Observe the output waveform noting the pulse amplitude and rise time. (If a calibrated 'scope is not available, recall the method of adjusting the 'scope voltage and time base settings to correspond to the 10 KHz, 8 volt amplitude Signal Generator pulse output with two pulses set on the scope as in Experiment 14, Page 2).

   Repeat the observation with Switch C UP and adjust the 100K POT for a good square wave. Sketch and enter the results below:

SWITCH C DOWN	OBSERVE PULSE Rise Time (1) = _____ Amplitude (1) = _____
SWITCH C UP (Compensation is in.)	Adjust 100K POT for Square Pulse Rise Time (2) = _____ Amplitude (2) = _____

3. Calculate the attentuation factor:

$$\text{ATTENTUATION} = \frac{\text{AMPLITUDE (2)}}{\text{AMPLITUDE (1)}}$$

ATTENTUATION =

ATTENUATION =

Ed-Lab | INDUCTIVE SHUNT COMPENSATION | EXP. NO. 50 Page No. 1

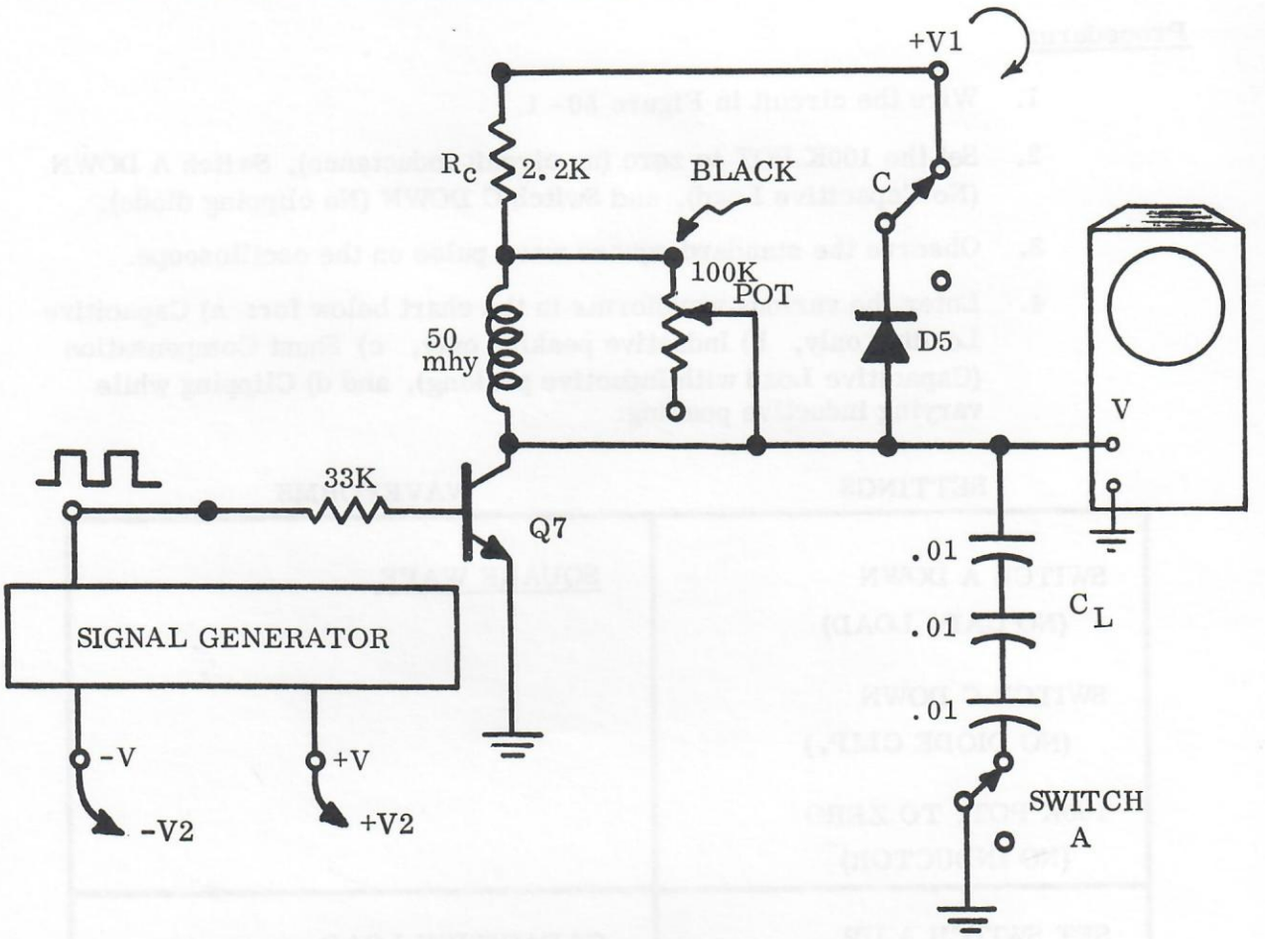


Figure 50-1 Inductor Shunt Compensation

Objective:

You will use an INDUCTOR for SHUNT PEAKING to improve rise-time for a Capacitive Load.

Description:

With Switch A DOWN, and the 100K POT set to zero, the above circuit is the same as in the previous experiment with the 2.2K collector resistor, R_c, and load capacitance, C_L, with a rise-time determined by the time constant, $R_C C_L$. This circuit then produces the same rise time for an output pulse as in the previous experiments. With the 100K POT set at 100K, an INDUCTOR is in series with the collector resistor, R_c, which for circuit analysis (neglecting the power supply) is really in parallel or SHUNT with the Capacitive load. The SHUNT INDUCTOR improves rise time. The Diode, D5, (through Switch C) is used to clip-off any overshoots caused by the inductance. The variation of the 100K POT enables us to vary the effect of the Inductor.

Procedure:

1. Wire the circuit in Figure 50-1.
2. Set the 100K POT to zero (no circuit inductance), Switch A DOWN (No Capacitive Load), and Switch C DOWN (No clipping diode).
3. Observe the standard square wave pulse on the oscilloscope.
4. Enter the various waveforms in the chart below for: a) Capacitive Loading only, b) Inductive peaking only, c) Shunt Compensation (Capacitive Load with Inductive peaking), and d) Clipping while varying inductive peaking:

SETTINGS	WAVEFORMS
SWITCH A DOWN (NO CAP. LOAD) SWITCH C DOWN (NO DIODE CLIP.) 100K POT. TO ZERO (NO INDUCTOR)	SQUARE WAVE
SET SWITCH A UP (CAPACITIVE LOAD)	CAPACITIVE LOAD
SET SWITCH A DOWN (NO CAP. LOAD) SET 100K POT TO MAXIMUM 100K (INDUCTOR PEAKING)	INDUCTOR PEAKING

Ed-Lab	INDUCTIVE SHUNT COMPENSATION	EXP. NO. 50 Page No. 3

SETTINGS	WAVE FORMS
ADJUST 100K POT FOR SINGLE PEAK	SINGLE PEAK PULSE VOLTAGE LEVEL = _____ PEAK VOLTAGE LEVEL = _____
SWITCH A UP (CAP. LOAD)	INDUCTIVE SHUNT COMPENSATION
KEEP SWITCH A UP SWITCH C UP (CLIPPING DIODE IN) VARY 100K POT	PULSE CLIPPING RISE TIME: (ZERO TO FULL LEVEL) = _____

Ed-Lab | DIGITAL to ANALOG CONVERTER | EXP. NO. 51 Page No. 1

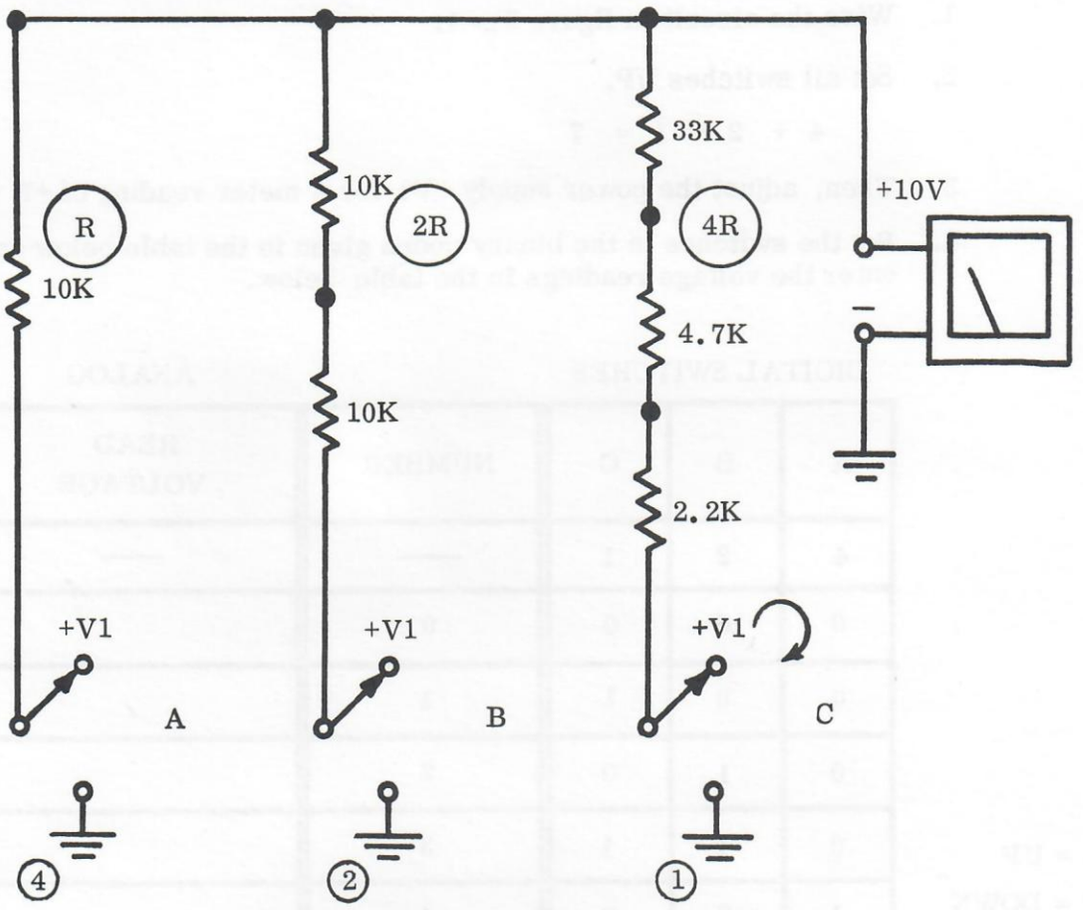


Figure 51-1 D to A Converter

Objective:

You will use 3 switches coded in a BINARY 4 2 1 CODE and a resistor network to yield a Digital to Analog Converter.

Description:

The three switches are coded with the binary "weights" 4, 2, 1. These are connected to resistors "weighted" as R 2R 4R (10K, 20K, 40K). The switches are connected to either +VOLTS or ground. The output "analog" voltage is proportional to the input "digital" switch settings.

Procedure:

1. Wire the circuit in figure 51 - 1.
2. Set all switches UP.

   4 + 2 + 1 = 7
3. Then, adjust the power supply +V1 for a meter reading of +7 volts.
4. Set the switches in the binary codes given in the table below and enter the voltage readings in the table below.

1 = UP

0 = DOWN

DIGITAL SWITCHES				ANALOG
A	B	C	NUMBER	READ VOLTAGE
4	2	1	——	——
0	0	0	0	
0	0	1	1	
0	1	0	2	
0	1	1	3	
1	0	0	4	
1	0	1	5	
1	1	0	6	
1	1	1	7	

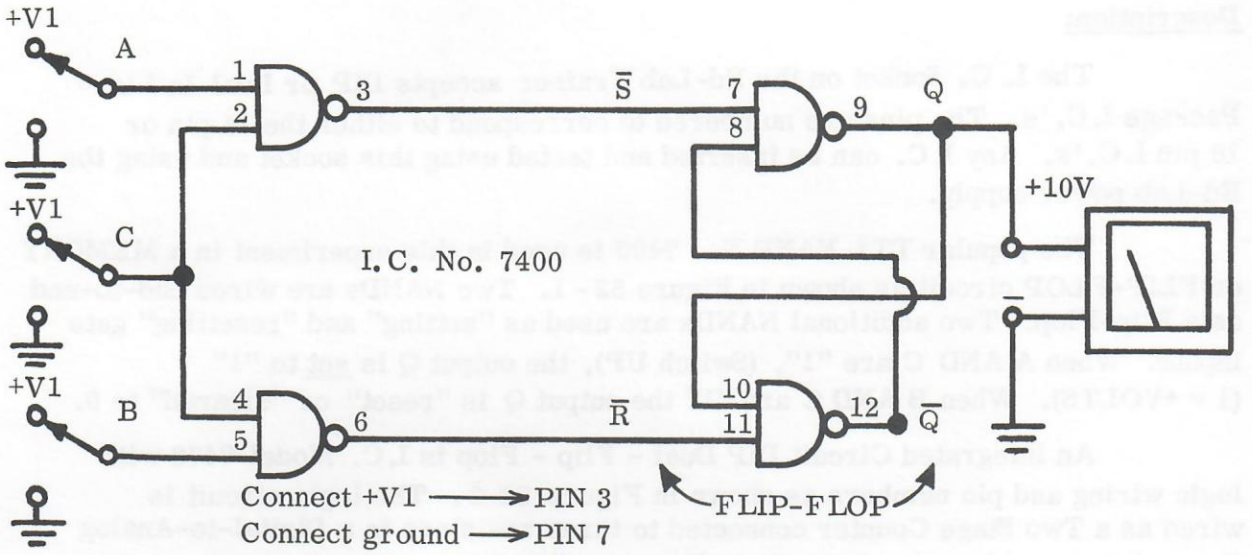


Figure 52-1 Set-Reset NAND FLIP-FLOP

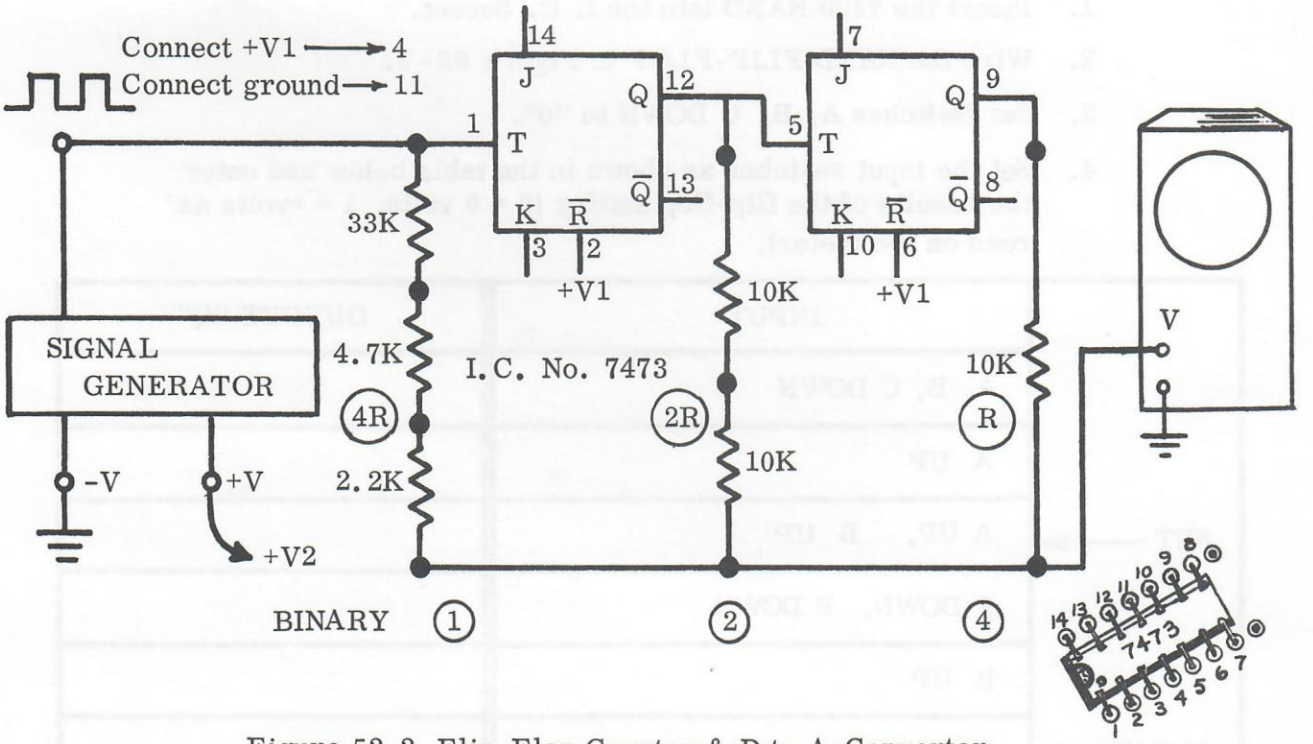


Figure 52-2 Flip-Flop Counter & D to A Converter

Objective:

You will use DIGITAL INTEGRATED CIRCUITS to implement a NAND SET-RESET FLIP-FLOP, and you will test a BINARY COUNTER with a D to A CONVERTER sweep circuit.

Description:

The I. C. Socket on the Ed-Lab Trainer accepts DIP or Dual-In Line-Package I.C.'s. The pins are numbered to correspond to either the 14 pin or 16 pin I.C.'s. Any I.C. can be inserted and tested using this socket and using the Ed-Lab power supply.

The popular TTL NAND No. 7400 is used in this experiment in a MEMORY or FLIP-FLOP circuit as shown in Figure 52-1. Two NANDs are wired end-to-end as a Flip-Flop. Two additional NANDs are used as "setting" and "resetting" gate inputs. When A AND C are "1", (Switch UP), the output Q is <u>set</u> to "1" (1 = +VOLTS). When B AND C are "1" the output Q is "reset" or "cleared" to 0.

An Integrated Circuit DIP Dual - Flip - Flop is I.C. Model 7473 with logic wiring and pin numbers as shown in Figure 52-2. The logic circuit is wired as a Two Stage Counter connected to three resistors in a Digital-to-Analog Converter network to provide a digitally controlled 8-step voltage.

Procedure:

1. Insert the 7400 NAND into the I. C. Socket.
2. Wire the NAND FLIP-FLOP in Figure 52-1.
3. Set Switches A, B, C DOWN to "0".
4. Set the input switches as shown in the table below and enter the results of the flip-flop setting (0 = 0 volts, 1 = +volts as read on the meter).

	INPUT	OUTPUT "Q"
	A, B, C DOWN	
	A UP	
SET →	A UP, B UP	
	A DOWN, B DOWN	
	B UP	
CLEAR →	B UP, C UP	
	A DOWN, B DOWN, C DOWN	
	B DOWN, A UP	
SET →	B DOWN, A UP, C UP	

5. Does the logic circuit operate as a Memory?

6. Remove the 7400 NAND I.C. and insert the DUAL FLOP-FLOP I.C. Number 7473.

7. Wire the Flip-Flop Counter and Digital to Analog Conversion System shown in Figure 52 - 2.

8. Observe the output "staircase waveform" on the oscilloscope and plot the results below:

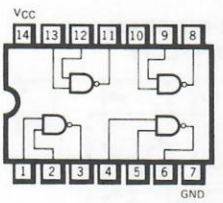
DIGITAL STAIRCASE WAVEFORM

TTL/SSI • 9N00/5400, 7400

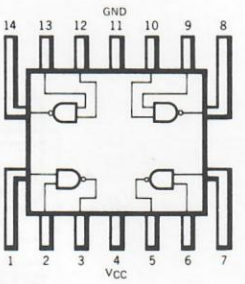
QUAD 2-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

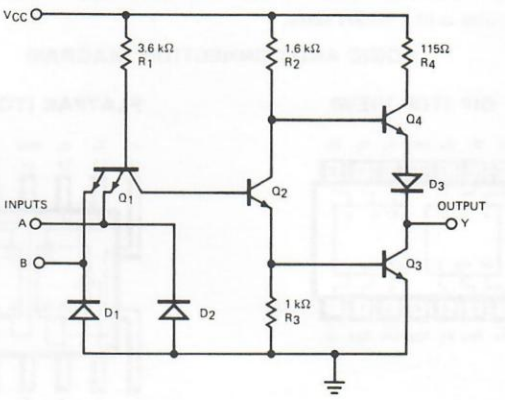


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{AB}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N00XM/5400XM			9N00XC/7400XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product..

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = 0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N00/5400	V_{CC} = MAX.	5
		–18		–55	mA	9N00/7400		
I_{CCH}	Supply Current HIGH		4.0	8.0	mA	V_{CC} = MAX., V_{IN} = 0V		6
I_{CCL}	Supply Current LOW		12	22	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Note more than one output should be shorted at a time.

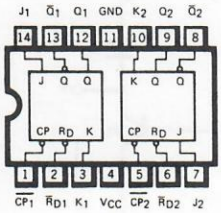
HIGH SPEED TTL/SSI • 9H73/54H73, 74H73

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS AND CLOCKS

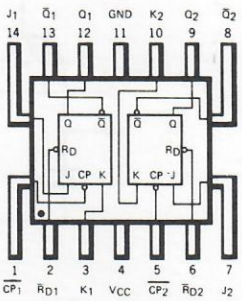
DESCRIPTION – The HSTTL/SSI 9H73/54H73, 74H73 is a High Speed Dual JK Master/Slave flip-flop with separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave. Logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



FLATPAK (TOP VIEW)

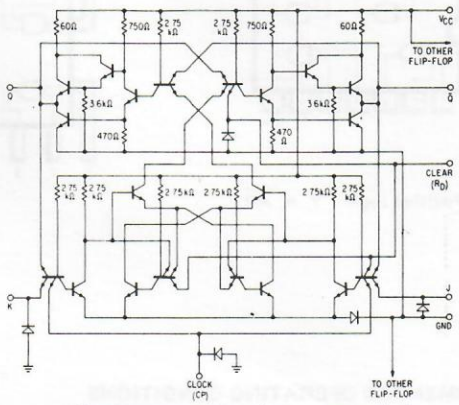


Positive logic:

LOW input to clear sets Q to LOW level

Clear is independent of clock

SCHEMATIC DIAGRAM (EACH FLIP-FLOP)



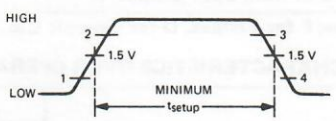
Component values shown are typical.
Resistor values are in ohms.

TRUTH TABLE

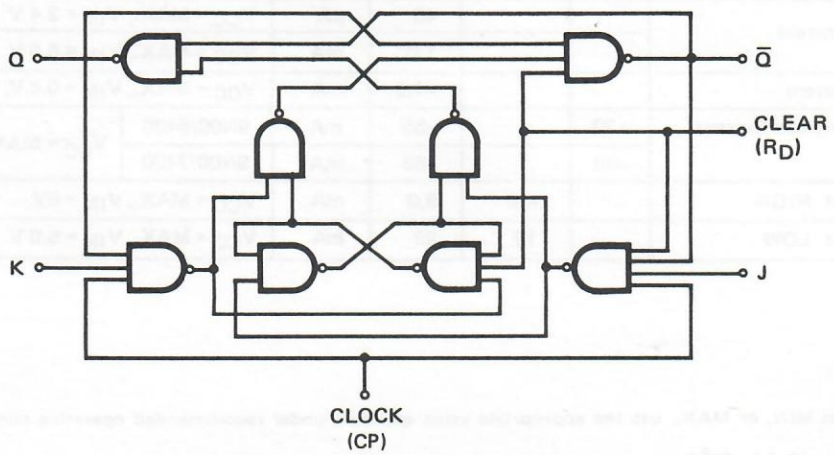
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORMS



LOGIC DIAGRAM (EACH FLIP-FLOP)



TTL/MSI 9393/5493, 7493

4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input $\overline{CP}_B$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input $\overline{CP}_B$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

		LOADING
R_0	Reset-Zero Input	1 U.L.
$\overline{CP}_A$	Clock (Active LOW going edge) Input	2 U.L.
$\overline{CP}_B$	Clock (Active LOW going edge) Input	2 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

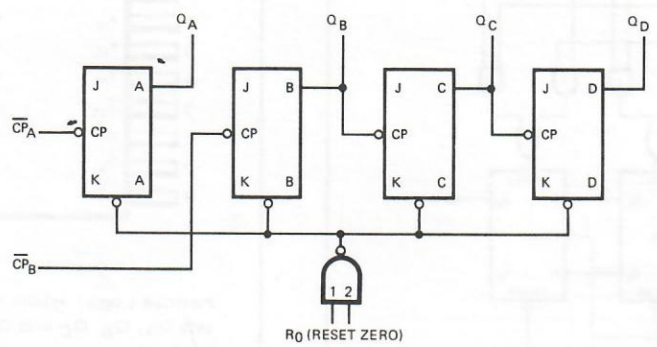
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE (See Notes 1, 2 and 3)

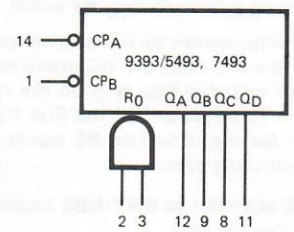
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES:
1. Output Q_A connected to input $\overline{CP}_B$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM

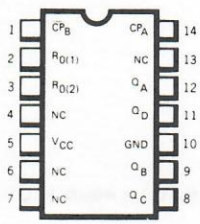


LOGIC SYMBOL

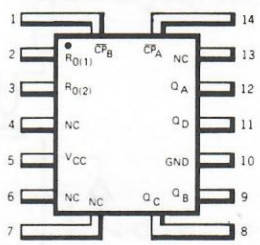


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No Internal Connection
Positive logic: See Truth Table

TTL/MSI 9394/5494, 7494

4-BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9394/5494, 7494 is composed of four RS master/slave flip-flops, four AND-OR-INVERT gates and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the LOW state by applying a HIGH level voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the HIGH state from either of two preset input sources. Preset inputs P_{1A} through P_{1D} are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a LOW level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs P_{2A} through P_{2D} are active.

Transfer of information to the outputs occurs when the clock input goes from a LOW to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input, preset 1, and preset 2 must be at a LOW state when clocking occurs.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

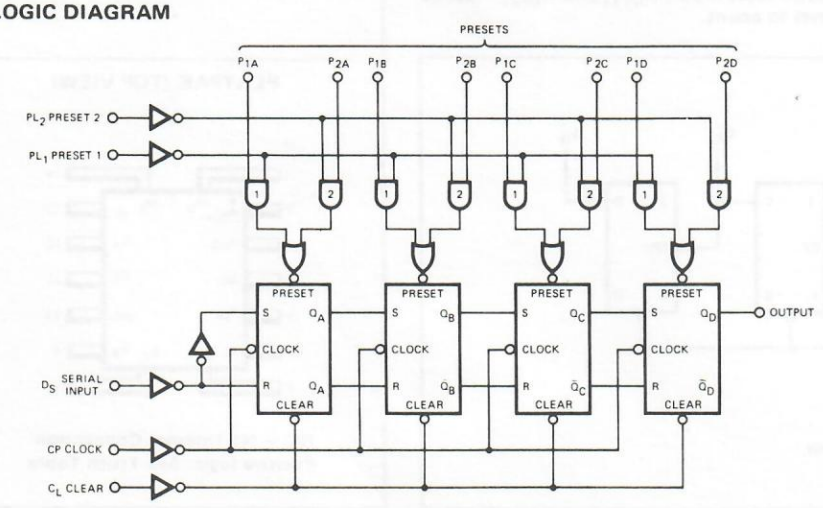
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

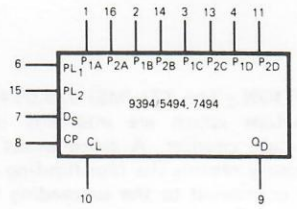
PIN NAMES		LOADING
$P_{1A} - P_{2D}$	Preset Inputs	1 U.L.
PL_1	Preset 1 Input	4 U.L.
PL_2	Preset 2 Input	4 U.L.
D_S	Serial Data Inputs	1 U.L.
CP	Clock Input	1 U.L.
C_L	Clear Input	1 U.L.
Q_D	Serial Data Output	10 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

LOGIC DIAGRAM

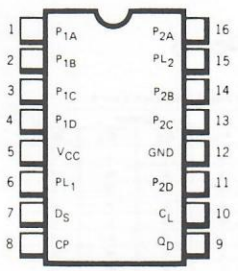


LOGIC SYMBOL

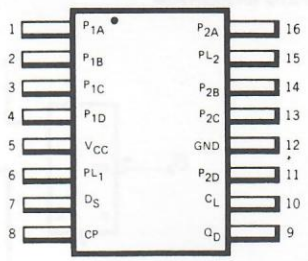


V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



FLAT PAK (TOP VIEW)



Positive Logic: HIGH input to clear sets Q_A, Q_B, Q_C and Q_D to LOW level.

TTL/MSI 9380/5480, 7480

GATED FULL ADDER

DESCRIPTION – The TTL/MSI 9380/5480, 7480 is a single-bit, high speed, Binary Full Adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial-carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

PIN NAMES

		LOADING
A_1, A_2, B_1, B_2	Non Inverting Data Inputs	1 U.L.
A*, B*	Inverting Data Inputs	1.65 U.L.
A_C, B_C	Control Inputs	1 U.L.
C_n	Carry Input	5 U.L.
$\overline{C_{n+1}}$	Carry Output	5 U.L.
Σ, $\overline{\Sigma}$	Sum Outputs	10 U.L.
A*, B*	When Used as Outputs	3 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

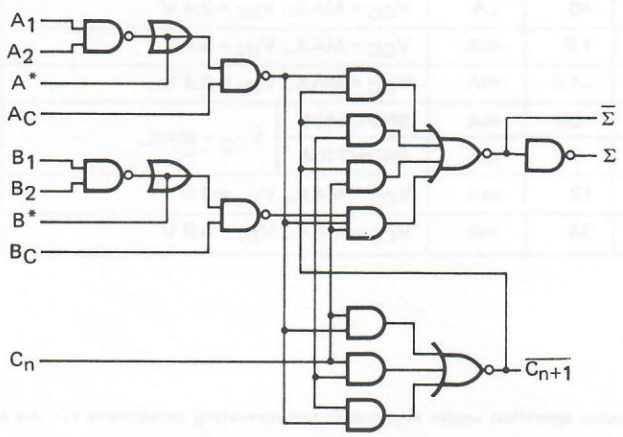
TRUTH TABLE

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

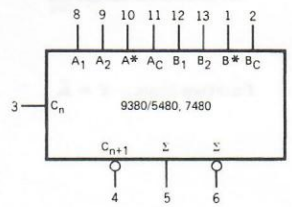
NOTES:

1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$. $B^* = \overline{B_1 \cdot B_2}$
2. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively must be open or used to perform Dot-OR logic.

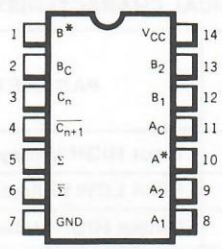
LOGIC DIAGRAM



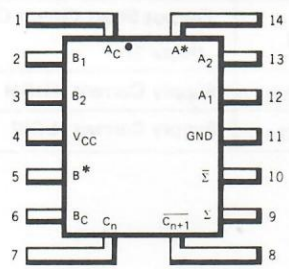
LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)



FLATPAK (TOP VIEW)



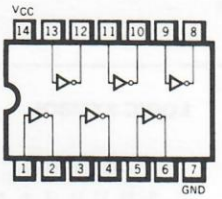
Positive logic: See truth table

TTL/SSI • 9N04/5404, 7404

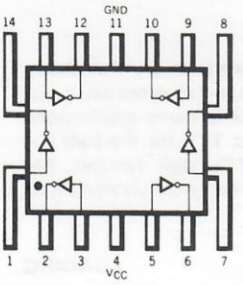
HEX INVERTER

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

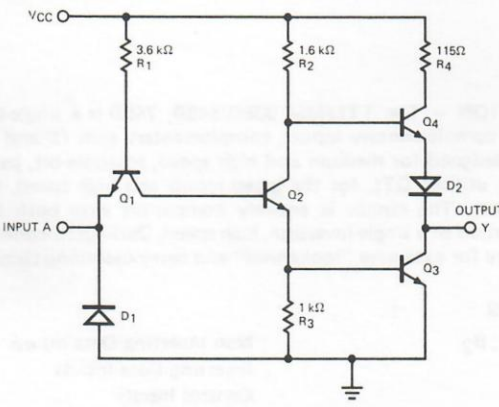


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{A}$

SCHEMATIC DIAGRAM (EACH INVERTER)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N04XM/5404XM			9N04XC/7404XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		15
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		16
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		16
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		15
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V		18
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		18
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N04/5404	V_{CC} = MAX.	19
		–18		–55	mA	9N04/7404		
I_{CCH}	Supply Current HIGH		6.0	12	mA	V_{CC} = MAX., V_{IN} = 0 V		20
I_{CCL}	Supply Current LOW		18	33	mA	V_{CC} = MAX., V_{IN} = 5.0 V		20

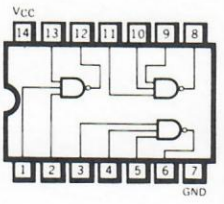
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TTL/SSI • 9N10/5410, 7410

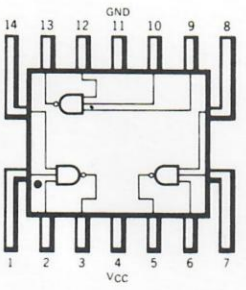
TRIPLE 3-INPUT NAND GATE

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)

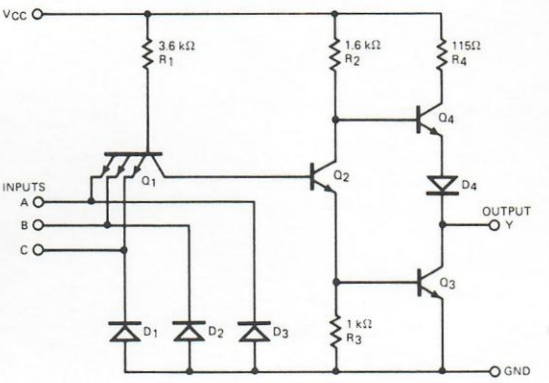


FLATPAK (TOP VIEW)



Positive logic: $Y = \overline{ABC}$

SCHEMATIC DIAGRAM (EACH GATE)



Component values shown are typical.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9N10XM/5410XM			9N10XC/7410XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA, V_{IN} = 0.8 V		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = 2.0 V		1
I_{IH}	Input HIGH Current			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V,	Each Input	3
I_{OS}	Output Short Circuit Current (Note 3)	–20		–55	mA	9N10/5410	V_{CC} = MAX.	5
		–18		–55	mA	9N10/7410		
I_{CCH}	Supply Current HIGH		3.0	6.0	mA	V_{CC} = MAX., V_{IN} = 0 V		6
I_{CCL}	Supply Current LOW		9.0	16.5	mA	V_{CC} = MAX., V_{IN} = 5.0 V		6

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

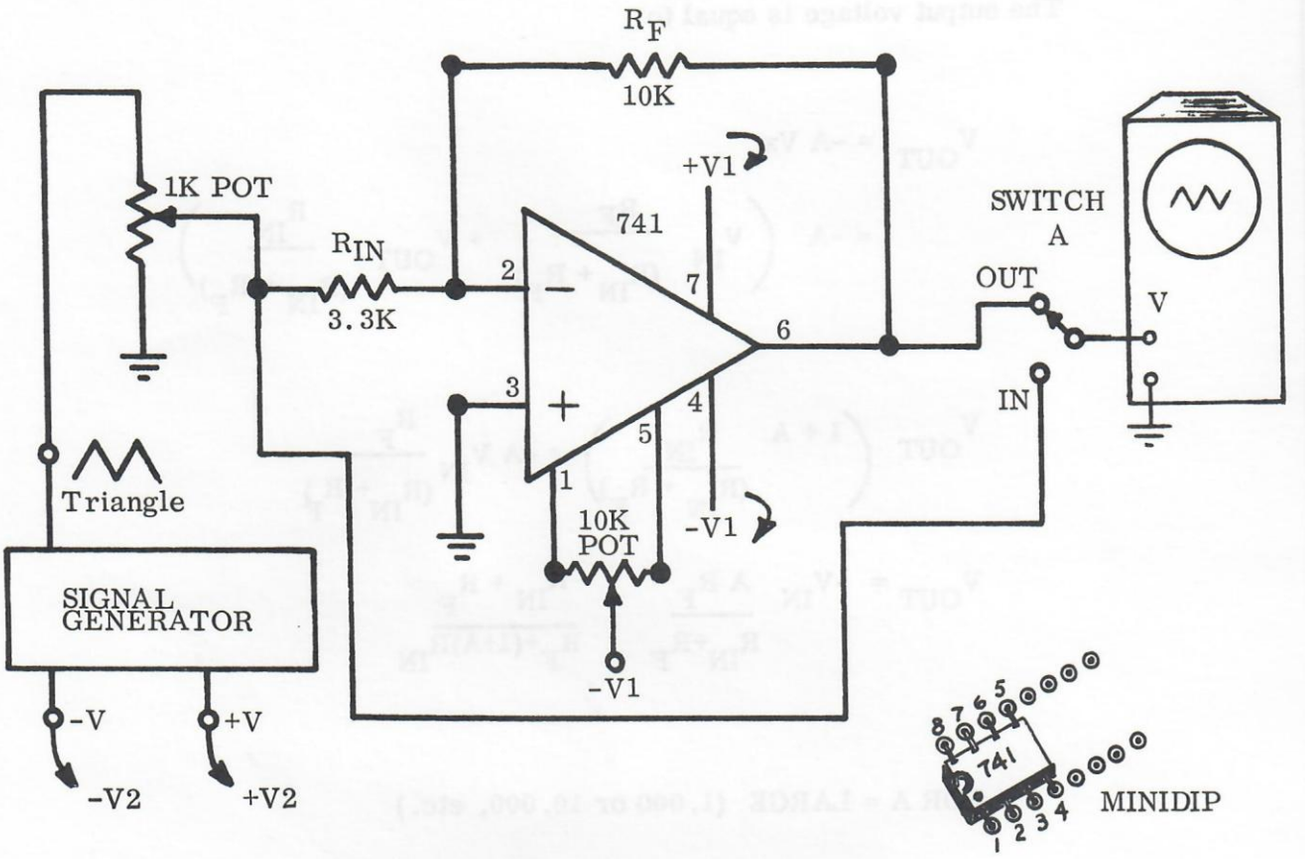


Figure 53-1 Operational Amplifier

Objective:

You will use a LINEAR INTEGRATED CIRCUIT Operational Amplifier in a Scaled Inverter Circuit.

Description:

Linear Integrated Circuits are ANALOG or varying voltage devices rather than DIGITAL or ON/OFF circuits. A typical Linear I.C. is the OPERATIONAL AMPLIFIER or DIFFERENCE AMPLIFIER. This circuit is usually a very High Gain Amplifier and is used with input and feedback resistors and components for computation and control and signal processing. An amplifier circuit is shown below with a fixed + input (ground) and with an input and feedback resistor connected to the - input.

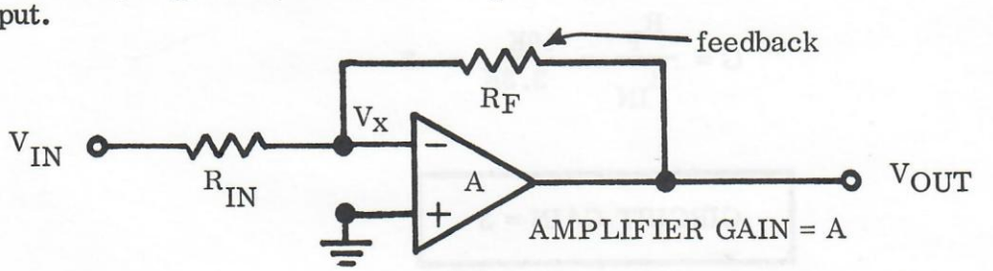


Figure 53-2 FEEDBACK OP-AMP

The output voltage is equal to:

$$V_{OUT} = -A\,Vx$$

$$= -A \left(V_{IN} \frac{R_F}{(R_{IN} + R_F)} + V_{OUT} \frac{R_{IN}}{(R_{IN} + R_F)} \right)$$

$$V_{OUT} \left(1 + A \frac{R_{IN}}{(R_{IN} + R_F)} \right) = -A\,V_{IN} \frac{R_F}{(R_{IN} + R_F)}$$

$$V_{OUT} = -V_{IN} \frac{A\,R_F}{R_{IN}+R_F} \quad \frac{R_{IN} + R_F}{R_F+(1+A)R_{IN}}$$

FOR A = LARGE (1,000 or 10,000, etc.)

$$V_{OUT} \approx -V_{IN} \frac{R_F}{R_{IN}}$$

The overall Gain (G) thus NEGATIVE and is given by

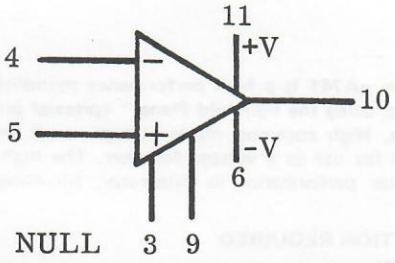
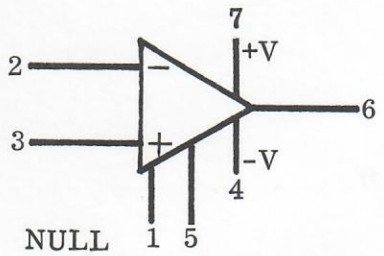
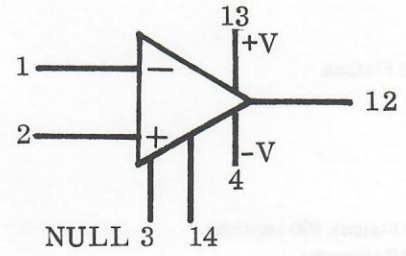
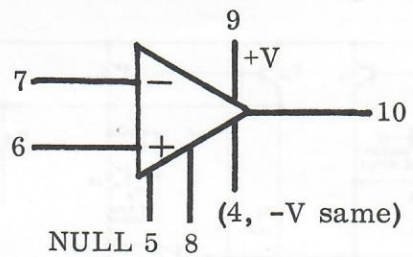
$$G = \frac{R_F}{R_{IN}}$$

FOR R_F= 10K and R_{IN} = 3.3K

$$G = \frac{R_F}{R_{IN}} = \frac{10K}{3.3K} = 3$$

CIRCUIT GAIN = 3

The OP-AMP used in this experiment is the model number 741. There are three different DIP (Dual-in-Line Package) Pin Layouts as summarized below:

14 PIN DIP 741	
8 PIN DIP 741	
14 PIN DIP TWO 741 (Model NO. 747)	 

The specification sheets for the 741 and 747 OP-AMPs are given on the following two pages.

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

LINEAR INTEGRATED CIRCUITS

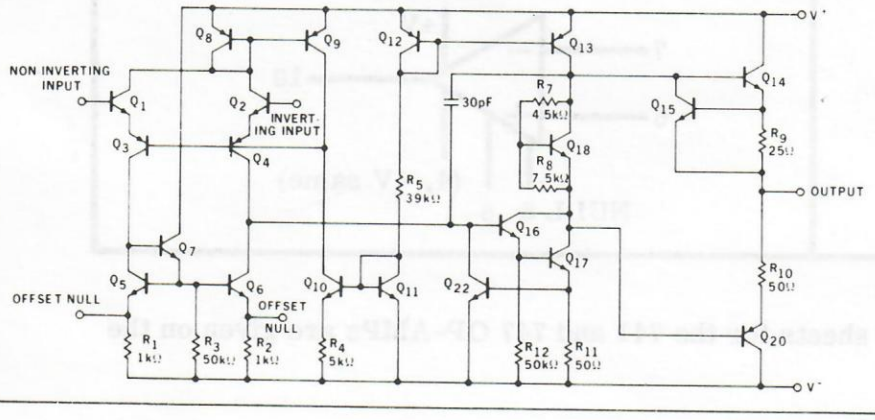
GENERAL DESCRIPTION – The μA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

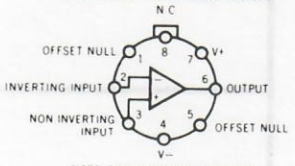
Supply Voltage	
Military (312 Grade)	±22 V
Commercial (393 Grade)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Mini DIP and Silicon DIP	−55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Lead Temperature (Soldering)	
Metal Can, Ceramic DIP and Flatpak (60 seconds)	300°C
Mini DIP and Silicone DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
(TOP VIEW)

8 LEAD METAL CAN

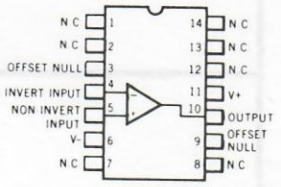


NOTE: PIN 4 CONNECTED TO CASE

ORDER PART NOS.

U5B7741312
U5B7741393

14 LEAD DIP



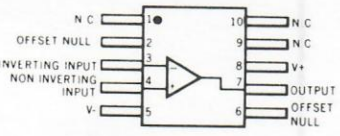
FOR CERAMIC DIP ORDER PART NOS.

U6A7741312
U6A7741393

FOR SILICONE DIP ORDER PART NO.:

U9A7741393

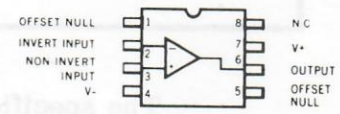
FLATPACK



ORDER PART NO.

U3F7741312

MINIDIP



ORDER PART NO.

U9T7741393

*Planar is a patented Fairchild process.

μA747

DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER

LINEAR INTEGRATED CIRCUITS

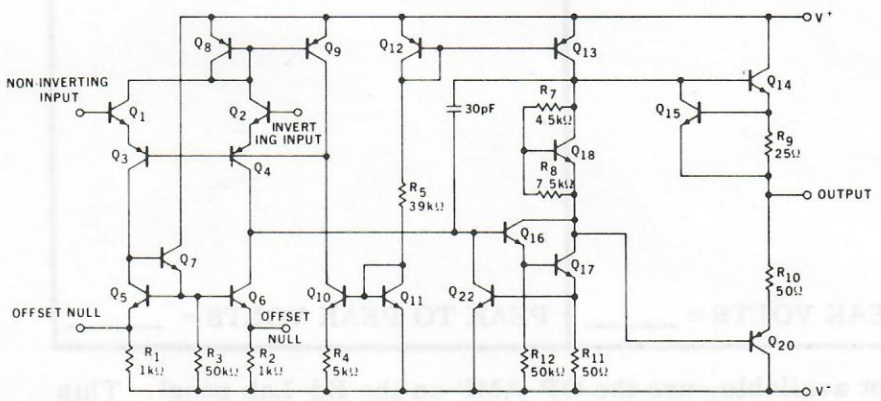
GENERAL DESCRIPTION – The μA747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

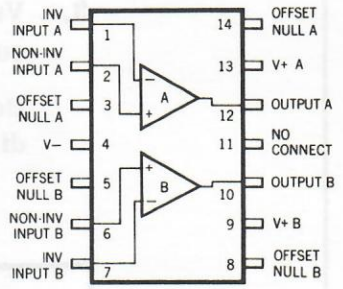
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (312 Grade)	±22 V
Commercial (393 Grade)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V⁻	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT (Each Side)

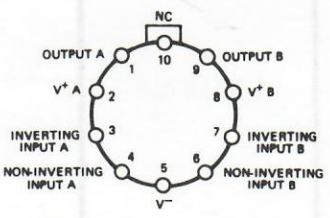


CONNECTION DIAGRAMS
(TOP VIEWS)
14 LEAD DIP



ORDER PART NOS.
U7A7747312
U7A7747393

10 LEAD METAL CAN



ORDER PART NOS.
U5F7747312
U5F7747393

*Planar is a patented Fairchild process.

Procedure:

1. Wire the circuit shown in Figure 53 - 1.* The pin numbers are given for the MINIDIP 8 pin DIP. If you are using the full-size DIP or the DUAL OP-AMP, substitute different pin numbers. Switch A is used to select the Output Voltage (UP), or the Input Voltage (DOWN).

2. Adjust the NULL OFF-SET POT (10K POT) by setting $V_{in} = 0$ by setting the V_{in} 1K POT to zero.

   Observe the output signal, Switch A UP. Momentarily remove one lead of the 10K feedback resistor and adjust the 10K POT for an output which corresponds to the balance where the scope output jumps up and down between maximum and minimum voltages.

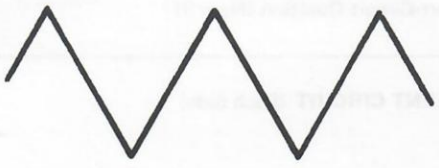
   Replace the 10K feedback resistor lead.

   The Null Off-Set is now adjusted.

3. Vary the input voltage to a convenient level and read the input and output voltage peak to peak levels on the oscilloscope.

   Be sure that the output and input triangle waveform is not clipped or distorted. Enter the data below:

WAVEFORMS

INPUT	OUTPUT
	
PEAK TO PEAK VOLTS = _____	PEAK TO PEAK VOLTS = _____

* If a 741 is not available, use the OP-AMP on the Ed-Lab panel. This internal Op-Amp has an internal null off-set. You can thus skip Step 2 above.

4. Calculate the system gain:

$$\text{GAIN} = \frac{V_{output}}{V_{input}} =$$

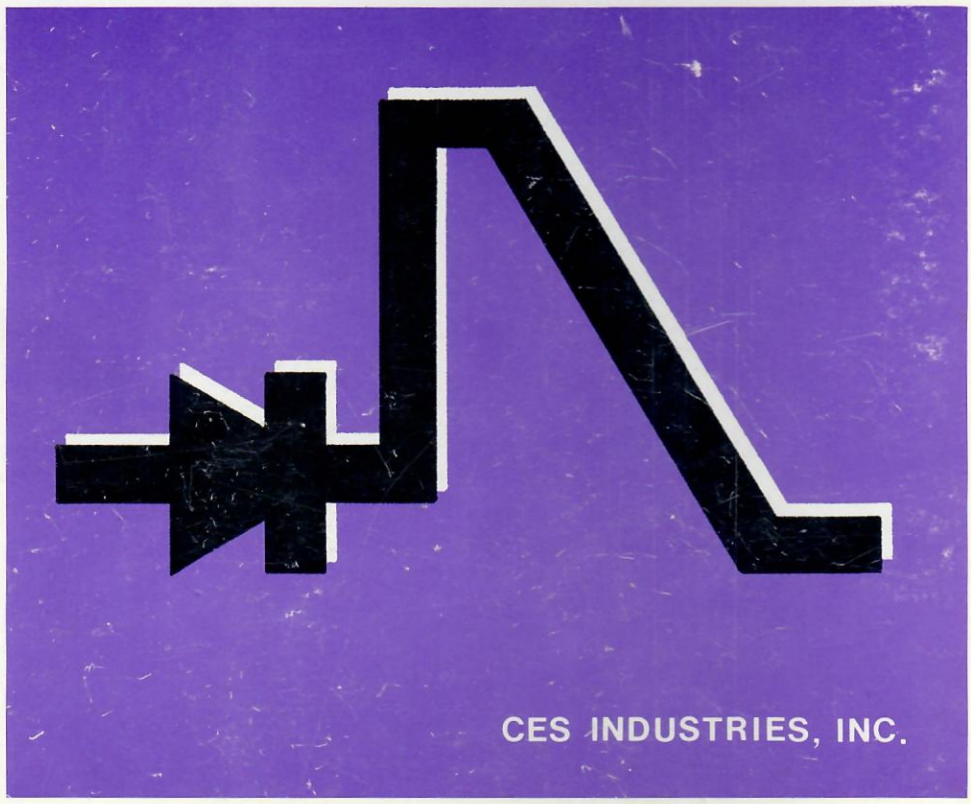
GAIN =

5. How does the MEASURED GAIN compare with the designed gain of -3? What is the output voltage variation range? What is the input voltage variation range?

6. What would the gain be for the following resistor combinations? Enter your calculation in the third column below:

R_{IN}	R_F	CALCULATE GAIN	MEASURE GAIN
3.3K	10K		
3.3K	3.3K		
3.3K	33K		
3.3K	100K		
3.3K	1K		
3.3K	100K POT		
10K	33K		
10K	1M POT		

7. Substitute the above resistors and measure the gain. How do the measured gains compare with the calculated gains?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